High Efficiency High Voltage 2A Step Down Converter

1 Features

- Wide 4.2V to 18V Input Voltage Range
- 2A Constant Output Current
- 250μA Low I_Q
- 0.6V Reference Voltage
- Integrated 113mΩ / 80mΩ MOSFETs
- 1.2MHz Switching Frequency
- Internal Soft-Start
- Pulse Frequency Mode at Light Load
- Cycle-by-Cycle Current Limit
- Hiccup Short Circuit Protection
- Thermal Shutdown Protection
- Available in SOT23-6 Package
- RoHS Compliant and Halogen-Free

2 Applications

- Security Cameras
- Flat Panels and Monitors
- Set Top Boxes and Media Players
- General Purpose

3 Description

The GD30DC1307-I12 is a high efficiency synchronous step-down switching converter. The device operates from an input voltage from 4.2V up to 18V. The main switch and synchronous switch are integrated in the device with very low R_{DS_ON} and capable of delivering up to 2A current.

The switching frequency is set at 1.2MHz to minimize output voltage ripple. Fault protection includes under voltage lockout, cycle-by-cycle current limit and thermal shutdown.

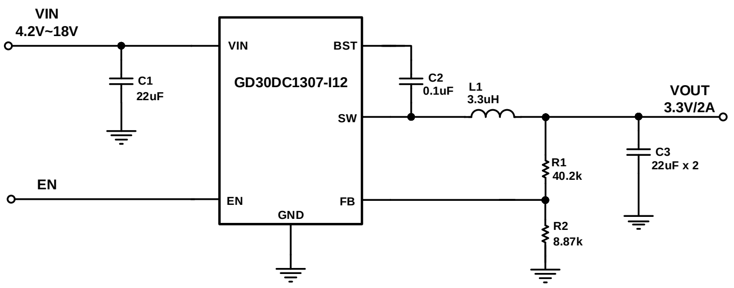
The GD30DC1307-I12 is available with space saving SOT23-6 package and requires minimal number of external components. Together with its low quiescent current, the GD30DC1307-I12 is ideal for security cameras, flat panels and monitors, digital set top boxes etc.

Device Information[1]

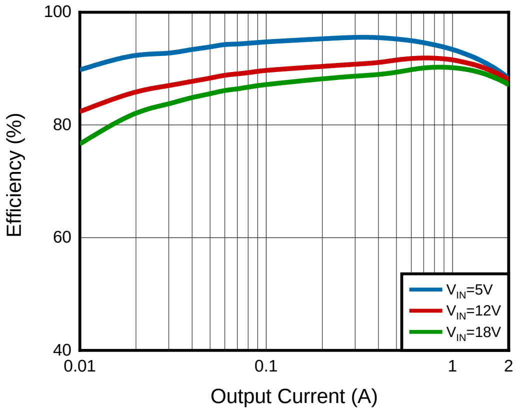
PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1307-I12	SOT23-6	2.92mm x 1.60mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



3.3V Output Efficiency



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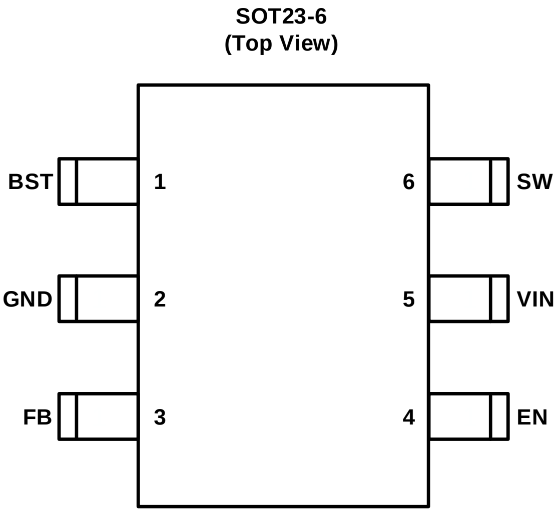
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	SOT23-6		
BST	1	O	**Bootstrap**. Connect a BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
GND	2	G	**Power ground.**
FB	3	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider.
EN	4	I	**Enable**. Pull high to enable the output.
VIN	5	P	**Power supply voltage**. Operates from a 4.2V to 18V input rail. A decoupling capacitor is required to decouple the input.
SW	6	O	**Switch output**. Switch pin connected to the internal MOSFET switches and inductor terminal.

1. I = Input, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	20	V
V_{EN}	Enable pin	–0.3	20	V
V_{BST}	Bootstrap voltage	–0.3	25	V
	Bootstrap(vs SW)	–0.3	6.5	V
V_{SW}	Switching node voltage	–0.3	20	V
	Switching node voltage(10ns transient)	–3	22	V
V_{FB}	Feedback pin	–0.3	6.5	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.2		18	V
V_{OUT}	Output voltage	0.9		$V_{IN} * D_{MAX}$	V
I_{OUT}	Output current	0		2	A
V_{IO}	I/O pin voltage(EN, FB)	0		5.5	V
T_J	Operating junction temperature	–40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	SOT23-6	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	117.71	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	59.55	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	34.00	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	59.46	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	2.27	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current	No switching	179	250	330	µA
I_{SHDN}	Shutdown current	V_{EN} = 0V	2	3	8	µA
T_{SS}	Soft-start time		0.9	1.5	2.0	ms
V_{UVLO}	Under voltage lockout	V_{IN} rising		4		V
V_{UVLO_HYS}	Under voltage lockout hysteresis			330		mV
ENABLE						
V_{EN_RISE}	Rising enable threshold		1.15	1.20	1.27	V
V_{EN_HYS}	Enable threshold hysteresis			150		mV
I_{EN}	Enable input current			2		µA
VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	V_{IN} = 4.2 to 18V, T_J=25°C	596	600	615	mV
I_{FB}	Feedback leakage current	T_J = –40°C to 125°C			50	nA
INTEGRATED POWER MOSFETS						
$R_{DS(on)}$	High-side FET on resistance			113		mΩ
	Low-side FET on resistance			80		mΩ
SWITCHING REGULATOR						
F_{SW}	Switching frequency	V_{FB} = 0.55V		1.2		MHz
I_{SW}	Switch node leakage current	V_{EN} = 0V, V_{IN} = 12V			10	µA
T_{ON_MIN}	Minimum on time[1]			58		nS
T_{OFF_MIN}	Minimum off time[1]			120		nS
I_{ZCD}	Zero-current detection[1]	V_{OUT} = 3.3V, L_O=4.7uH, I_{OUT} = 0A		60		mA
D_{HICCUP}	Hiccup duty cycle[1]			25		%
CURRENT LIMIT						
I_{LIM}	Valley current limit[1]			3.2		A

Electrical Characteristics (Continued)

V_{IN} = 12V, T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWM						
T_{TSD}	Thermal shutdown temperature[1]			150		°C
T_{HYS}	Thermal shutdown hysteresis[1]			20		°C

1. Guaranteed by design and engineering sample characterization.

5.6 Typical Characteristics

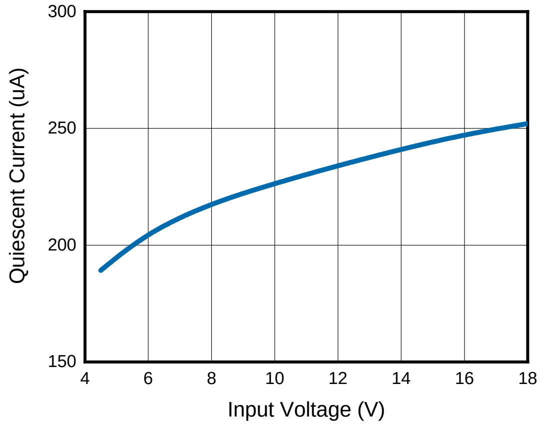


Figure 1. Quiescent Current vs. Input Voltage

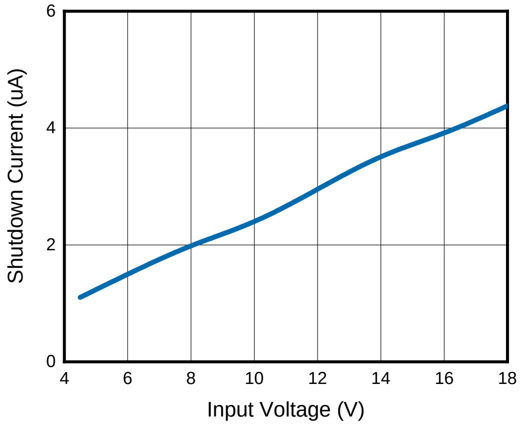


Figure 2. Shutdown Current vs. Input Voltage

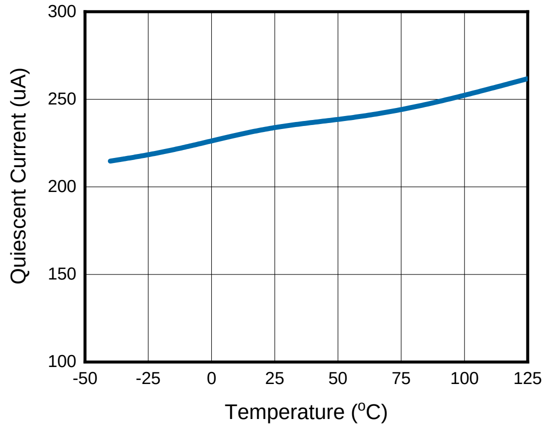


Figure 3. Quiescent Current vs. Temperature

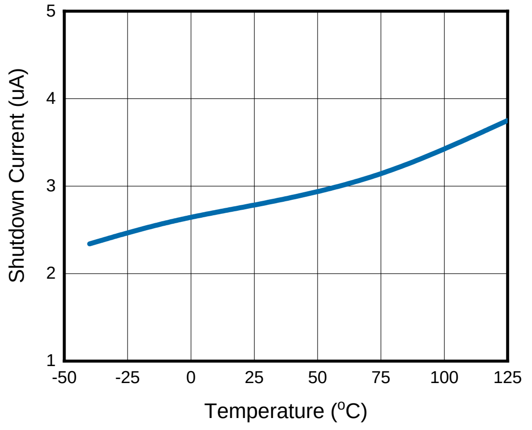


Figure 4. Shutdown Current vs. Temperature

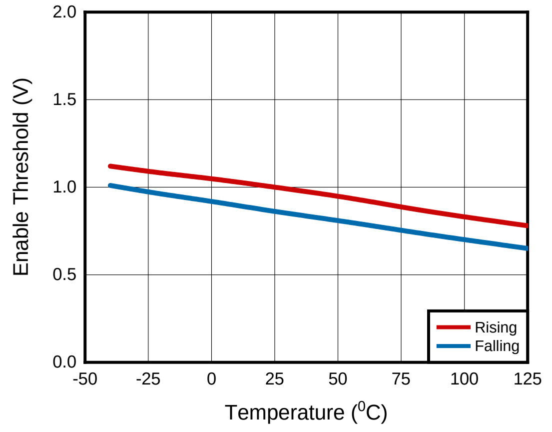


Figure 5. EN UVLO vs. Temperature

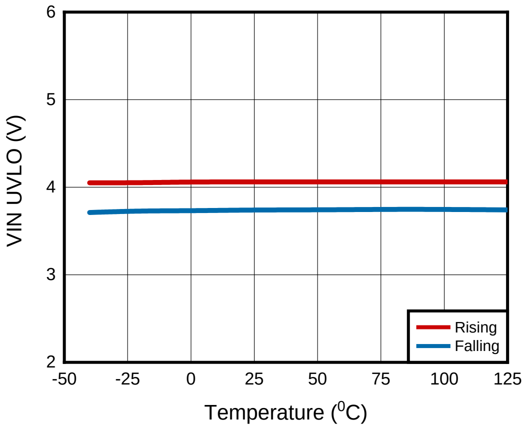


Figure 6. VIN UVLO vs. Temperature

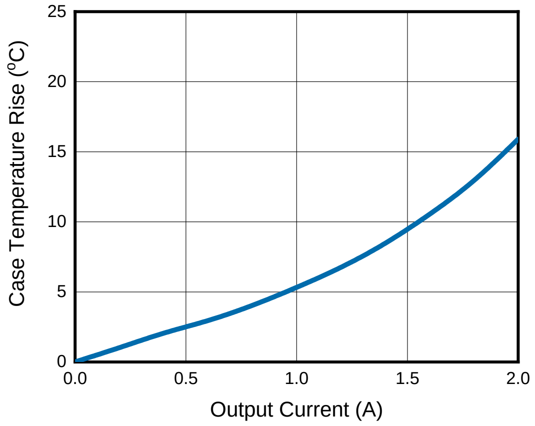


Figure 7. Temperature Rise vs. Temperature

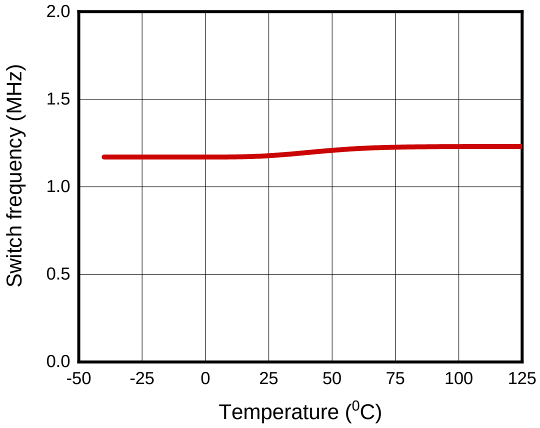


Figure 8. Switch Frequency vs. Temperature

6 Functional Description

6.1 Block Diagram

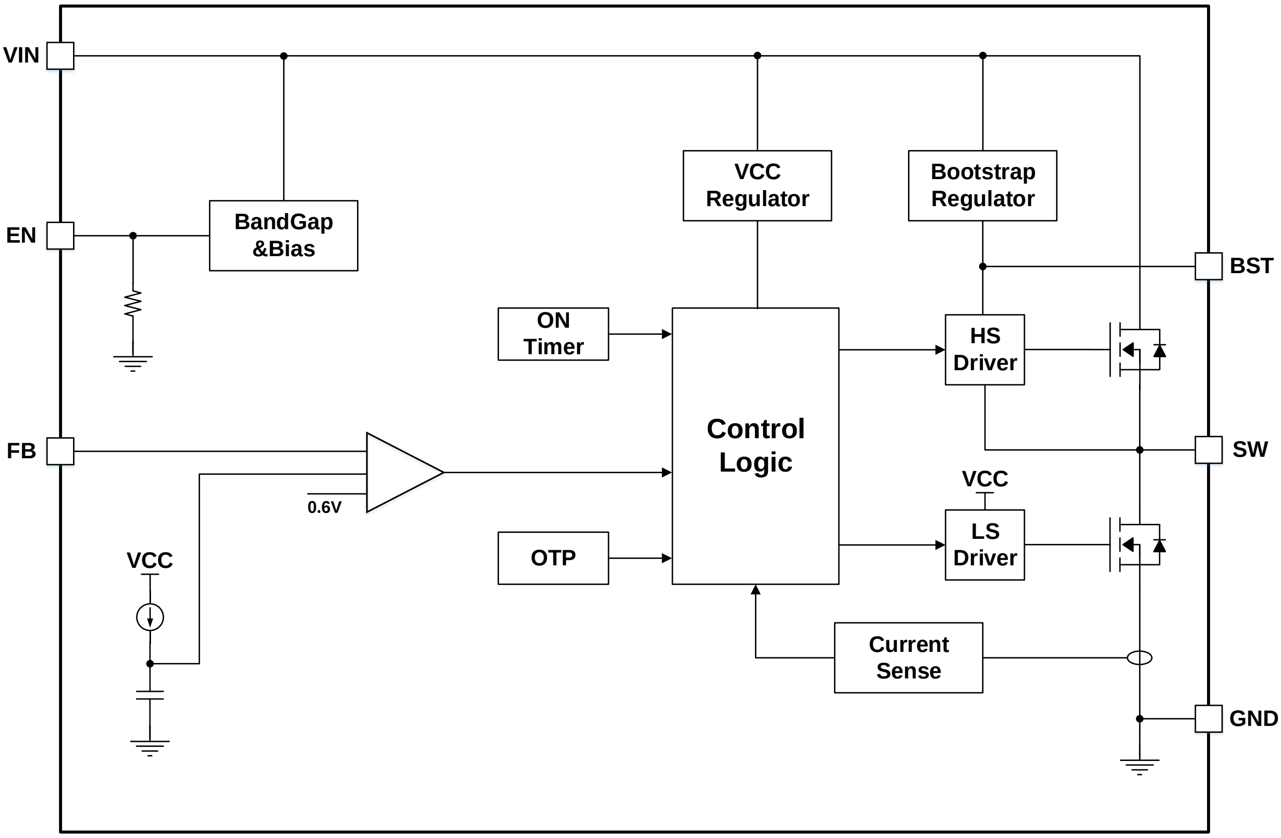


Figure 9. GD30DC1307-I12 Functional Block Diagram

6.2 Operation

The GD30DC1307-I12 is a synchronous switching DC/DC converter with constant on-time control. The adaptive on-time is so controlled by the input/output voltage that the IC operates at relative constant frequency, typically 1.2MHz. It is capable of delivering up to 2A for VIN between 4.2V and 18V. The output voltage can be as low as 0.9V.

6.2.1 Constant On-Time Control

Based on the V_{OUT}/V_{IN} ratio, a simple circuit sets the required on time for the high-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current. The relation between t_{ON} and V_{IN} and V_{OUT} is defined as following Equation(1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 0.83uS \tag{1}$$

Excellent load transient response is achieved with a unique fast response constant on-time valley current mode. The switching frequency changes during load transition so that the output voltage comes back in regulation faster than a traditional fixed PWM control scheme. Internal loop compensation is integrated which simplifies the design process while minimizing the number of external components.

6.2.2 Pulse Frequency Modulation

The GD30DC1307-I12 automatically operates with pulse frequency modulation (PFM) at light load currents. As the output current decreases, the GD30DC1307-I12 reduces the switching frequency to maintain high efficiency. When the inductor current reaches zero, the low-side MOSFET turns off. Then the output capacitors offer power for load and feedback resistors.

When feedback voltage(V_{FB}) drops below the reference voltage, the high-side MOSFET is turned on. As the output current increases, the time period that the current modulator regulates becomes shorter, and the high-side MOSFET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with the following Equation(2):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \qquad (2)$$

6.2.3 Soft Startup

After enabling the device, internal soft-start circuitry monotonically ramps up the output voltage which reaches nominal output voltage during a soft-start time of 1.5ms (typical). This avoids excessive inrush current and creates a smooth output voltage rise slope.

6.2.4 Pre-Bias Startup

The GD30DC1307-I12 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

6.2.5 Bootstrap Charging

An external bootstrap capacitor can supplies the high-side MOSFET driver. This high-side driver has its own UVLO protection. The rising threshold is 2.2V(typical) and a hysteresis is 150mV(typical).VIN regulates the bootstrap capacitor voltage through a diode. The bootstrap regulator maintain a 4.5V(typical) voltage across BST-SW.

6.2.6 Under Voltage Lockout

To avoid mis-operation of the device at low input voltages, the GD30DC1307-I12 shuts down at voltages lower than 4V(typical) with hysteresis 330mV(typical).

6.2.7 Short Circuit Protection

The device provides short circuit protection function to prevent the device damaged from short condition. When the short condition occurs and the feedback voltage drops lower than 40% of the regulation level, the oscillator frequency will be reduced and hiccup mode will be triggered to prevent the device from overheating during the extended short condition. Once the short condition is removed, the frequency and current limit will return to normal.

6.2.8 Over Current Protection

The device has a 3.2A(typical) valley current limit control. While the low-side MOSFET is turned on, the conduction current is monitored by the internal circuitry. During over current protection(OCP) mode, the inductor valley current is exceeded the low-side source current limit, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the inductor valley current is below the low-side sourcing current-limit at the start of a cycle.

6.2.9 Short Circuit Protection

The GD30DC1307-I12 enters short-circuit protection mode when it reaches the current limit and attempts to recover with hiccup mode. In this process, the GD30DC1307-I12 disables the output power stage, discharges the soft-start capacitor, and then attempts to soft-start again automatically. If the short-circuit condition remains after the soft-start ends, the GD30DC1307-I12 repeats this cycle until the short-circuit disappears and the output rises back to regulation level, the hiccup time typically 7ms.

6.2.10 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 150°C(typical), both the high-side and low-side FETs are turned off. Once the device temperature falls below the threshold with hysteresis 20°C (typical), the device returns to normal operation automatically.

6.3 Device Mode Description

6.3.1 Device Enable

Enable (EN) is a digital control pin that turns the regulator on and off. Drive EN high to turn on the regulator; drive EN low to turn off the regulator. An internal 1MΩ resistor from EN to GND allows EN to be floated to shut down the chip. EN is clamped internally using a 2.8V series Zener diode (see Figure 10). Connecting the EN input through a pull-up resistor to the voltage on VIN limits the EN input current below 100μA, preventing damage to the Zener diode.

For example, if connection 12V to VIN, then $R_{PULLUP} \geq (12V – 2.8V) / (100K\Omega + 840K\Omega) = 9.8\mu A$

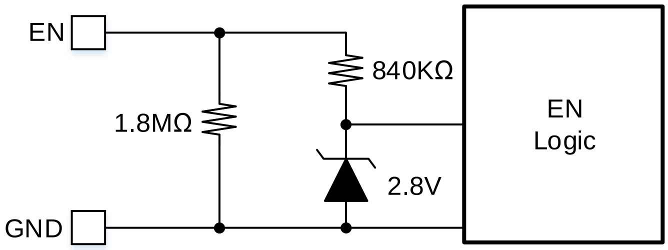


Figure 10. Zener Diode between EN and GND

7 Application Information

The GD30DC1307-I12 device is typically used as a step down converter, which convert an input voltage from 4.2V to 18V to fixed output voltage 3.3V.

7.1 Typical Application Circuit

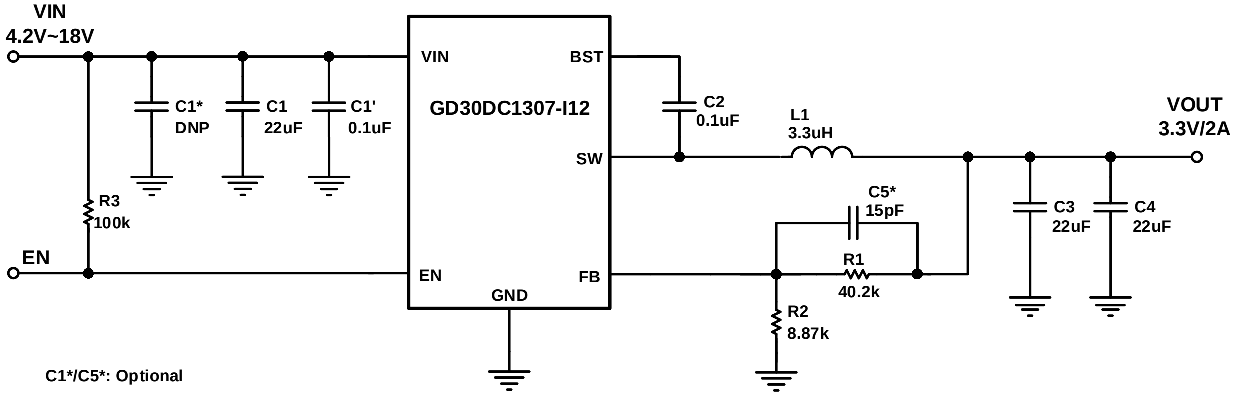


Figure 11. 3.3V, 2A Reference Design

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	4.2V to 18V
Output Voltage	3.3V
Maximum Output Current	2A

Table 2 lists the components used for the example.

Table 2. Design Example Component[1,2]

COMPONENT	DESCRIPTION
C1,C3,C4	22μF, Ceramic Capacitor, 50V, X7R, size 0805
C2	0.1μF, Bootstrap Capacitor, 10V, X7R, size 0603
L1	4.7μH, Power Inductor
R1,R2,R3	Divider resistor, 1%, size 0603
C5*	Optional, 15pF if it is needed

1. The components used in these design cases do not belong to GD products, GD does not warrant its accuracy or completeness. GD's customers need to test and verify whether the selected components meet their intended use to ensure stable system operation.
2. Refer to *Detailed Design Description* section for guidance on component selection and calculation equations.

7.3 Detailed Design Description

7.3.1 Output Voltage Setting

An external resistor divider is used to set output voltage according to Equation(3). By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage reference at the FB pin is 0.6V.

To ensure system performance, choose the value of R2 carefully. Since a large R2 make FB sensitive to noise and a small R2 increase power loss. So the value of 5KΩ-100KΩ is recommended. It can achieves a balance between system stability and low current consumption.

$$V_{OUT} = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \tag{3}$$

The feedback circuit is shown in Figure 12.

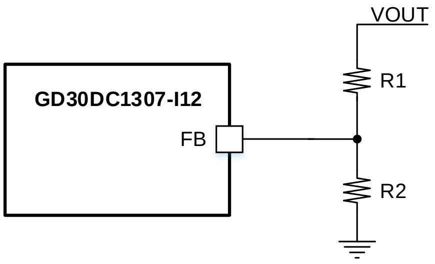


Figure 12. Feedback resistor divider

Table 3 lists the recommended parameters values for common output voltages.

Table 3. Component selection for common output voltages

V_{OUT}(V)	R1(KΩ,1%)	R2(KΩ,1%)	L(μH)
5.0	40.2	5.49	3.3
3.3	40.2	8.87	3.3
2.5	40.2	12.7	2.2
1.8	40.2	20	2.2
1.2	40.2	40.2	1.5
1.0	40.2	60.4	1.5
0.9	40.2	80.6	1

7.3.2 Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, inductors with larger inductance and low DCR values provide much more output and high conversion efficiency, and smaller inductance values can give batter load transient response.

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 40% of the IC rated current. And the peak inductor current can be calculated by Equation(4) and Equation(5). Ensure that the peak inductor current is below the maximum switch current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(MAX)} \tag{4}$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \tag{5}$$

The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value according to Equation(6). Once an inductor value is chosen, the peak inductor current is determined by Equation(5). Attention that the inductor should not saturate under the inductor peak current.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \tag{6}$$

7.3.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The input capacitance value determines the input voltage ripple of the converter. For most applications, a 10μF capacitor is sufficient.

The peak-to-peak voltage ripple on input capacitor can be estimated with Equation(7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \tag{7}$$

For best performance, ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To compensate the derating of the ceramic capacitors, the voltage rating of capacitor should be twice of the maximum input voltage. The input capacitor also requires an adequate ripple current rating since it absorbs the input switching current.

The input ripple current can be estimated with Equation(8):

$$I_{CIN} = I_{OUT} \times \sqrt{D \times (1 - D)} \tag{8}$$

Where D is the duty cycle of converter. The worst-case condition occurs at $V_{IN} = 2V_{OUT}$. At this point, the input ripple current of input capacitance is equal to half of output current. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

7.3.4 Output Capacitor Selection

The output capacitor stabilizes the DC output voltage, it directly affects the steady state, output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient.

The output voltage ripple can be estimated with Equation(9):

$$\Delta V_{OUT} = \Delta I_L \times \left(C_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \tag{9}$$

The output capacitor ripple is essentially composed of two part. One part is caused by the inductor ripple current flowing through the ESR of output capacitors, another part is caused by the inductor ripple current charging and discharging output capacitors. For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. And when using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

The output capacitance must be large enough to supply the current when a large load step occurs. But if the output capacitor value is too high, the output voltage will not be able to reach the design value during the soft start time. Two 22uF ceramic capacitors are recommended in this application.

7.4 Power Dissipation

For DC/DC, these is still some power deposited on the chip and converted into heat, in spite of switch mode power supplies have considerably higher efficiency when compared to linear regulators. The device power dissipation includes conduction loss, switching loss, gate charge loss and quiescent current losses. The maximum allowable continuous power dissipation at any ambient temperature is calculated by Equation(10):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \tag{10}$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance. Once exceeding the maximum allowable power, The device enters thermal shutdown to avoid permanent damage.

7.5 Typical Application Curves

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH, T_A = 25°C, unless otherwise noted.

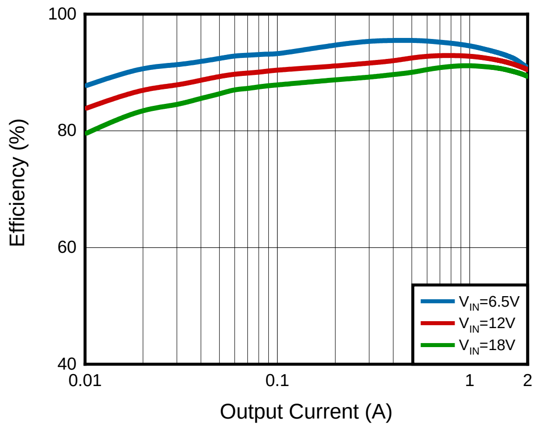


Figure 13. 5.0V Output Efficiency(DCR=27.3mΩ)

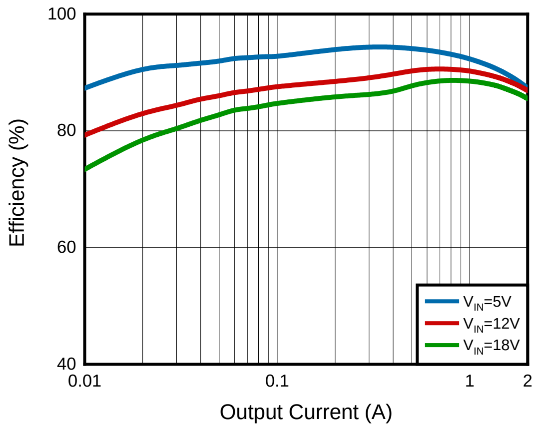


Figure 14. 3.3V Output Efficiency(DCR=27.3mΩ)

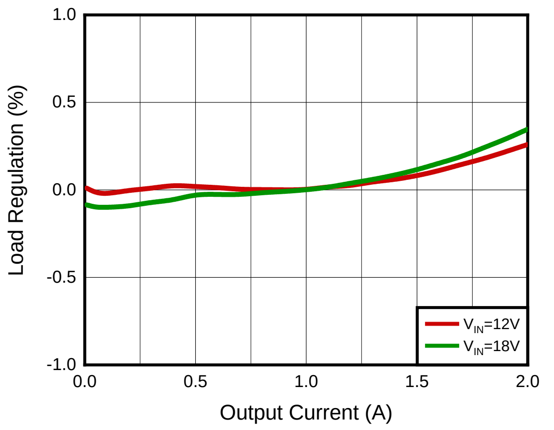


Figure 15. 5.0V Load Regulation

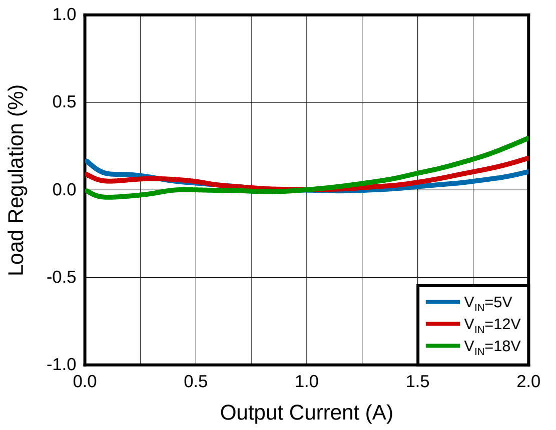


Figure 16. 3.3V Load Regulation

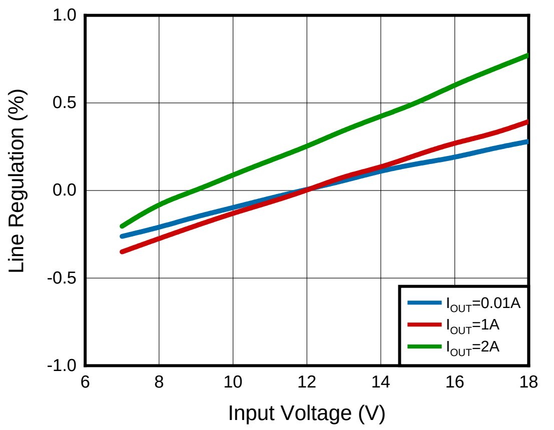


Figure 17. 5.0V Line Regulation

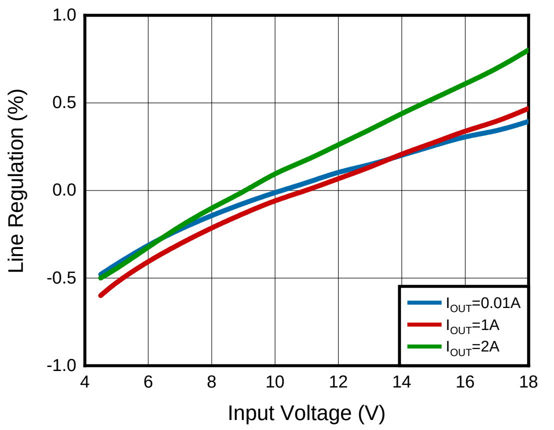
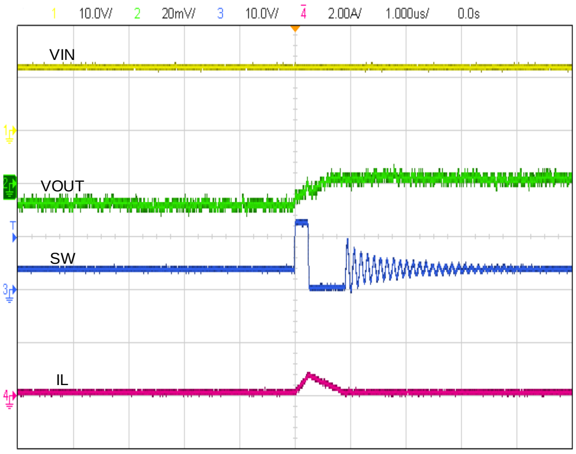


Figure 18. 3.3V Line Regulation

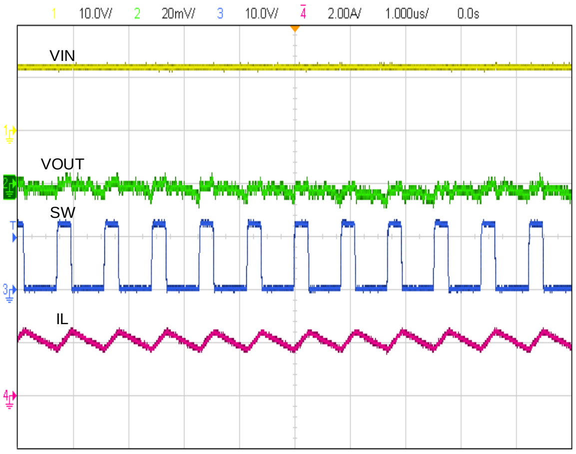
Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7µH, T_A = 25°C, unless otherwise noted.



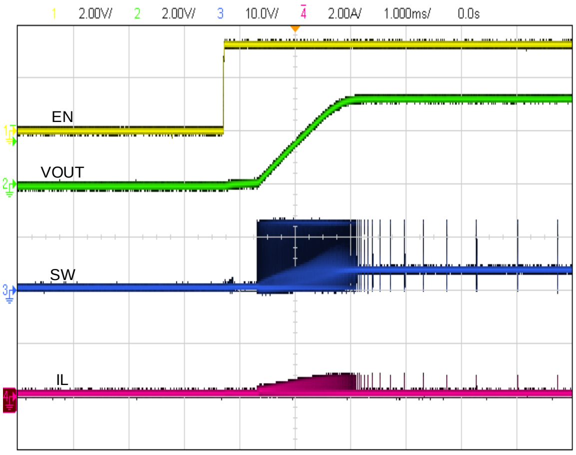
I_{OUT} = 0A

Figure 19. Output Ripple



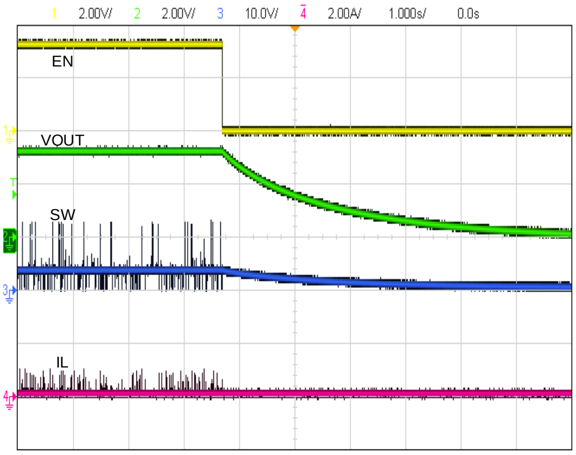
I_{OUT} = 2A

Figure 20. Output Ripple



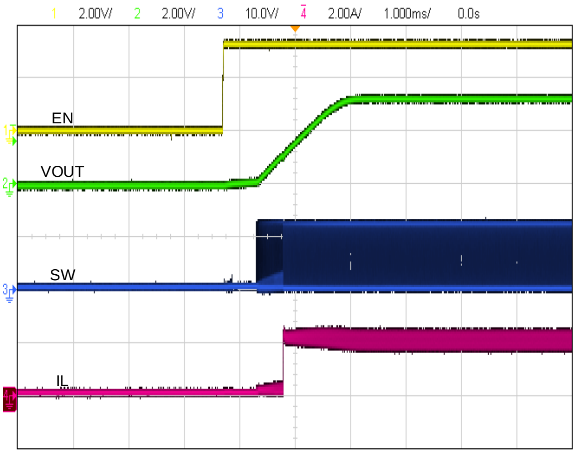
I_{OUT} = 0A

Figure 21. EN StartUp without Load



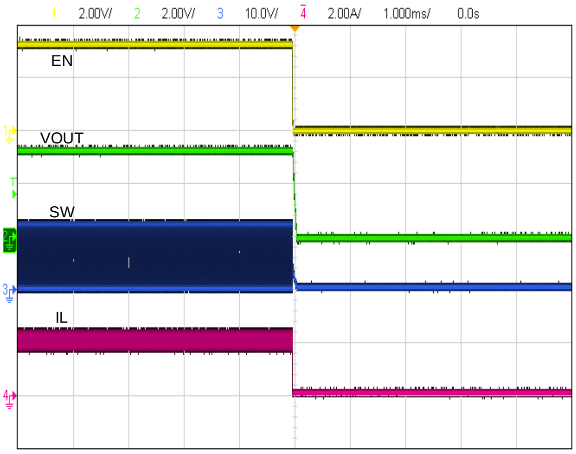
I_{OUT} = 0A

Figure 22. EN ShutDown without Load



I_{OUT} = 2.0A

Figure 23. EN StartUp with Load

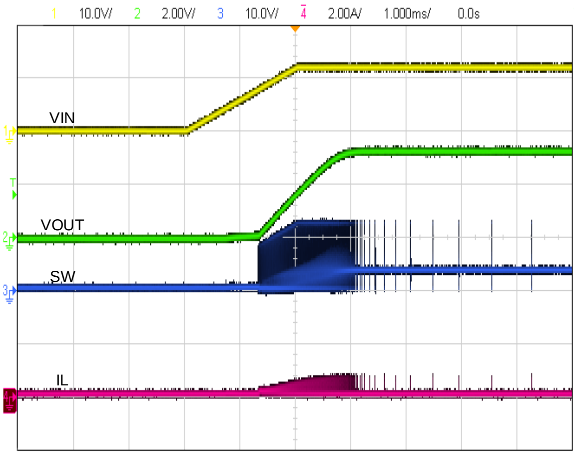


I_{OUT} = 2.0A

Figure 24. EN ShutDown with Load

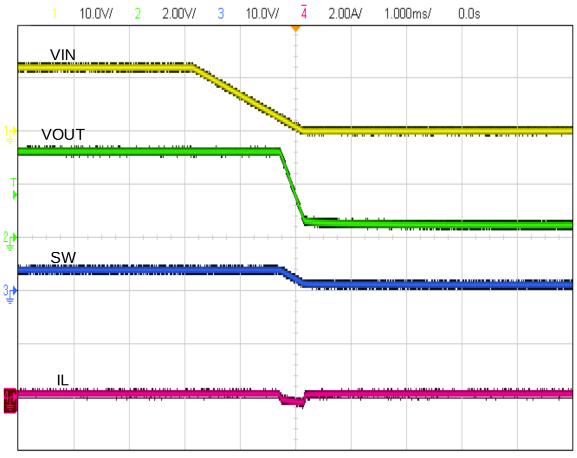
Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH, T_A = 25°C, unless otherwise noted.



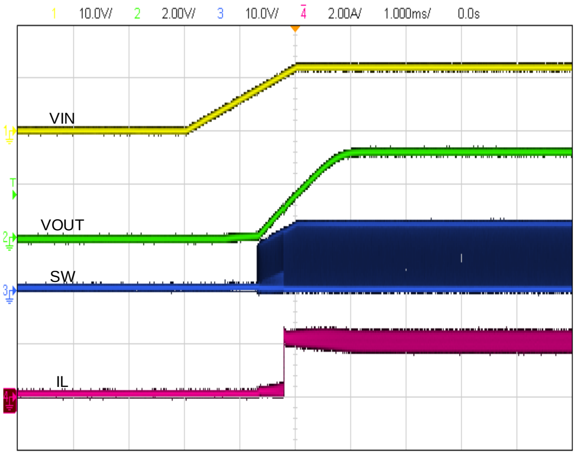
I_{OUT} = 0A

Figure 25. VIN StartUp without Load



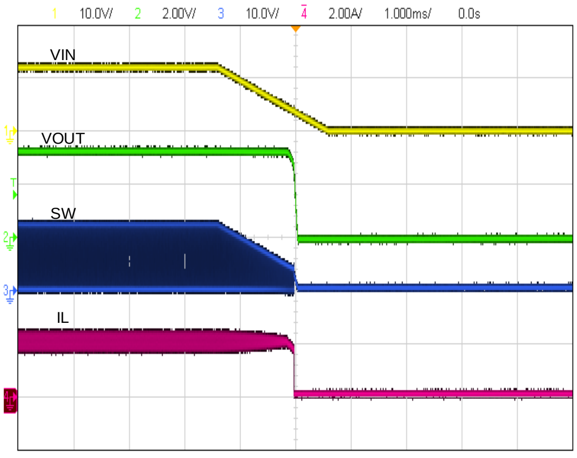
I_{OUT} = 0A

Figure 26. VIN ShutDown without Load



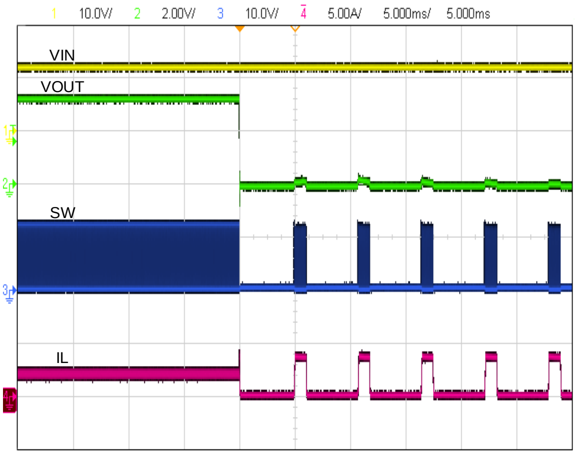
I_{OUT} = 2.0A

Figure 27. VIN StartUp with Load



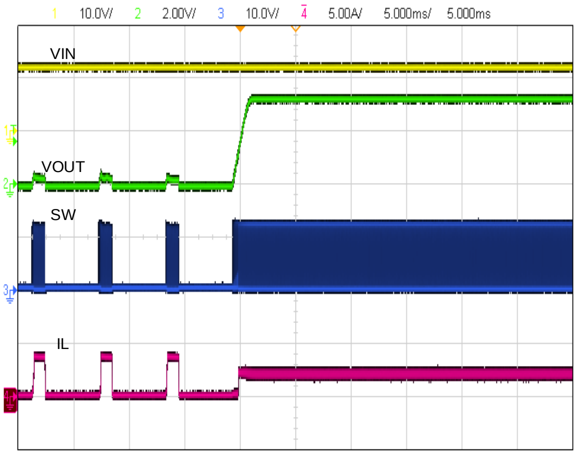
I_{OUT} = 2.0A

Figure 28. VIN ShutDown with Load



I_{OUT} = 2.0A

Figure 29. SCP Entry

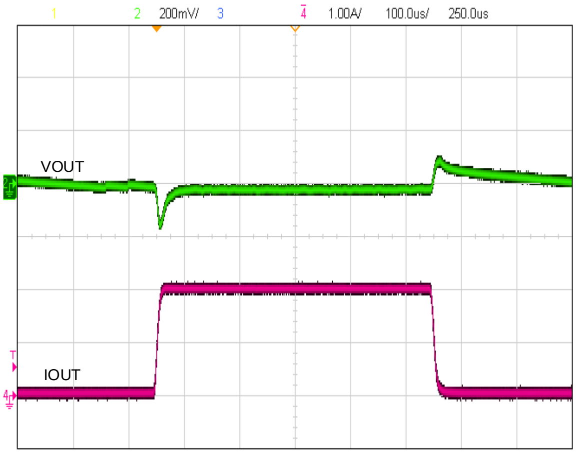


I_{OUT} = 2.0A

Figure 30. SCP Recovery

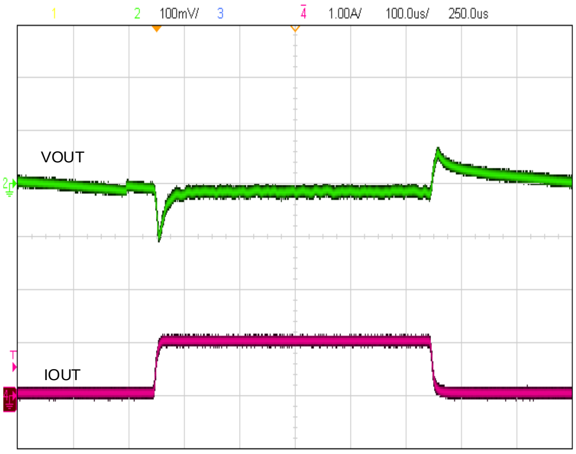
Typical Application Curves (continued)

V_{IN} = 12V, V_{OUT} = 3.3V, L = 4.7μH, T_A = 25°C, unless otherwise noted.



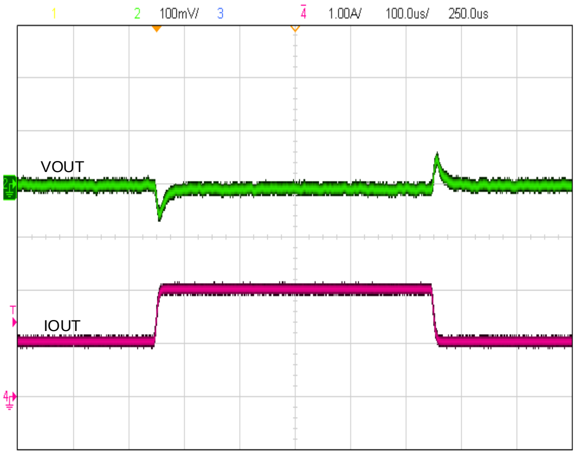
I_{OUT} = 0A to 2A, 2.5A/us slew rate

Figure 31. Load Transient



I_{OUT} = 0A to 1A, 2.5A/us slew rate

Figure 32. Load Transient



I_{OUT} = 1 A to 2A, 2.5A/us slew rate

Figure 33. Load Transient

8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues. For best results, follow the guidelines below.

1) Place the high-current paths (GND, IN, and SW) very close to the device with short, direct, and wide traces.
2) Place the input capacitor as close to IN and GND as possible.
3) Place the external feedback resistors next to FB.
4) Keep the switching node SW short and away from the feedback network.
5) Keep the VOUT sense line as short as possible or keep it away from the power inductor.

For best results, follow the layout example below.

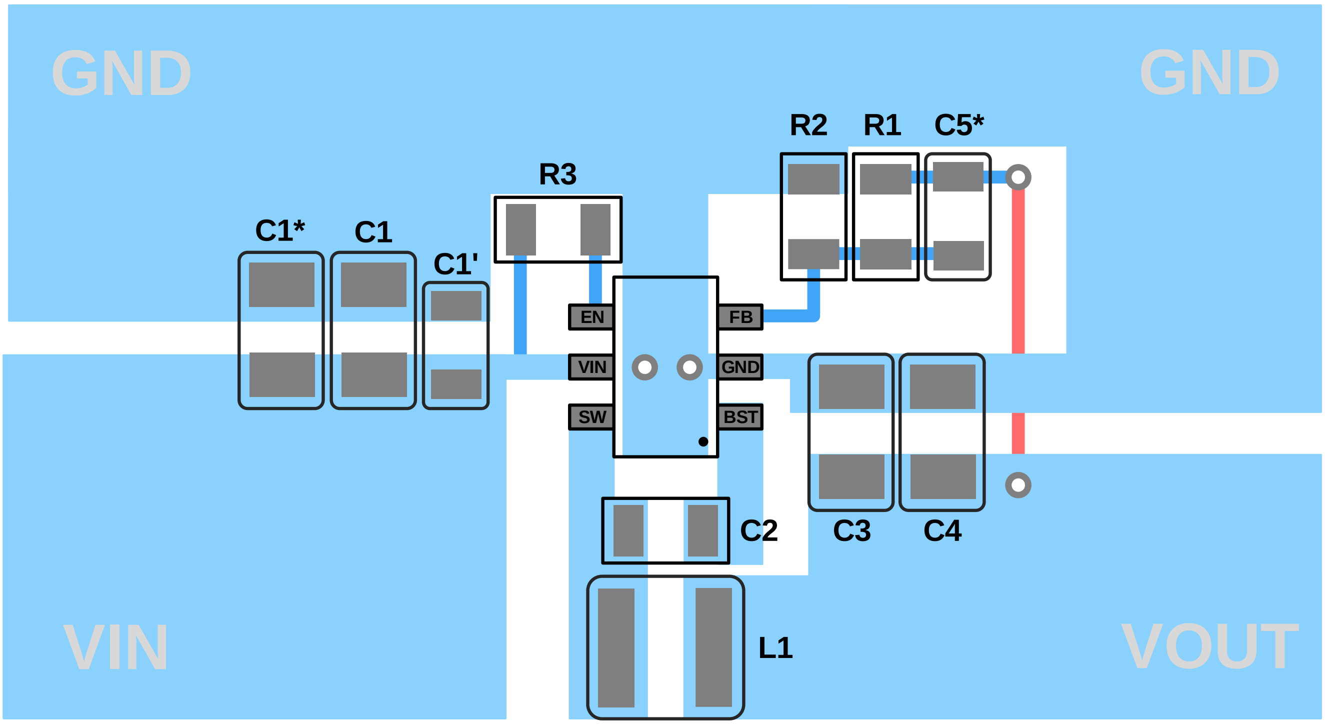
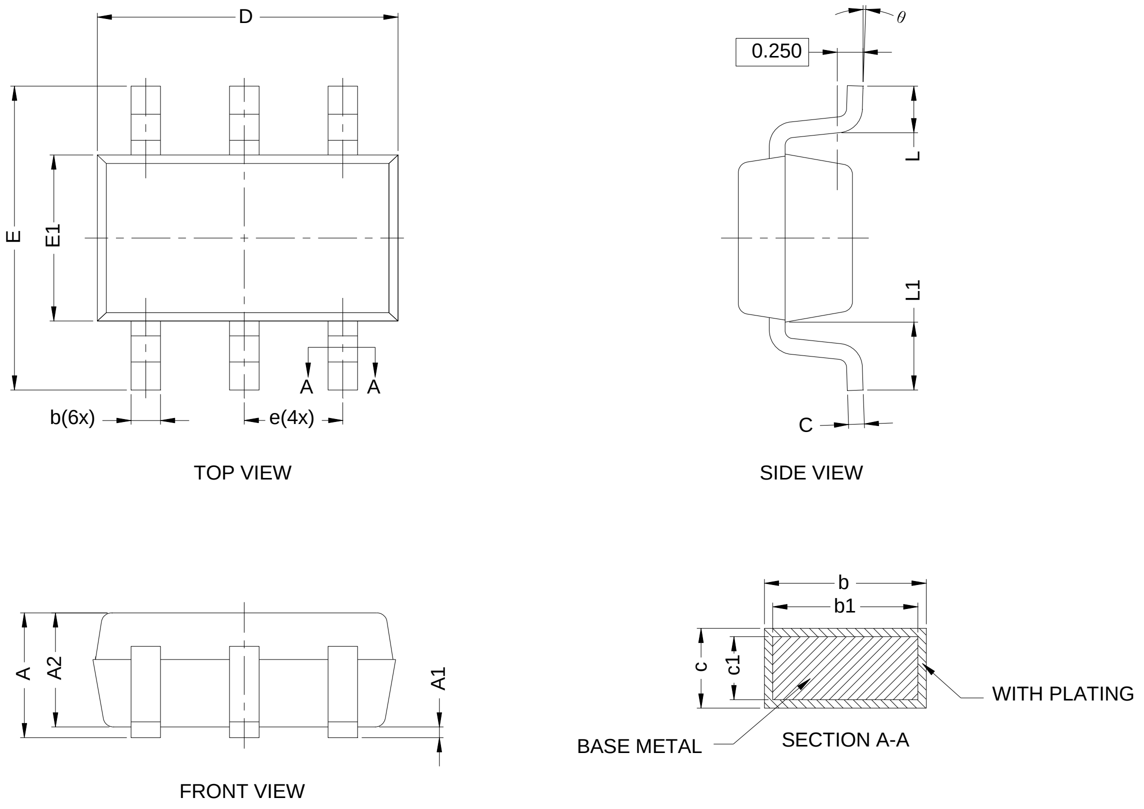


Figure 34. Typical GD30DC1307-I12 Example Layout

9 Package Information

9.1 Outline Dimensions

SOT23-6 Package Outline



NOTES:

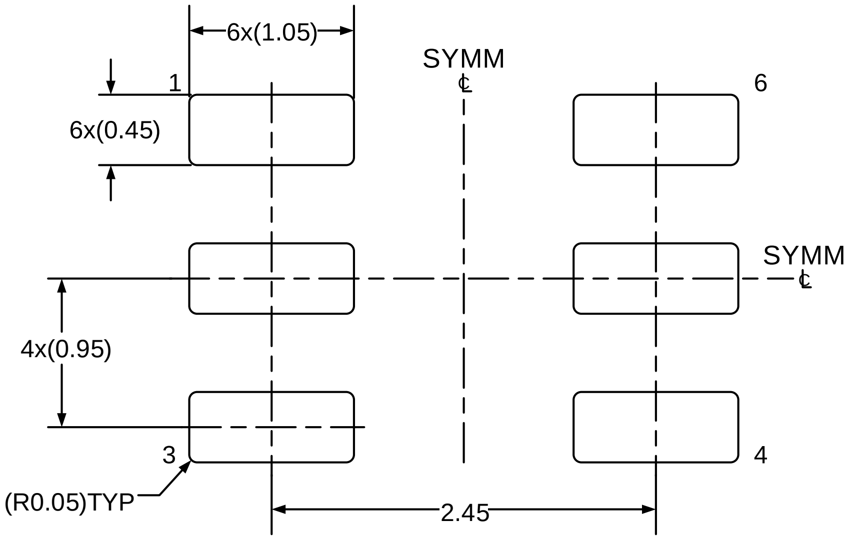
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 4 *SOT23-6 dimensions(mm)*.

Table 4. SOT23-6 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.25
A1	0.04		0.10
A2	1.00	1.10	1.20
b	0.38		0.46
b1	0.37	0.40	0.43
c	0.13		0.17
c1	0.12	0.13	0.14
D	2.82	2.92	3.02
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30		0.60
L1	0.60 REF		
θ	0°		8°

9.2 Recommended Land Pattern

SOT23-6 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1307SSTR-I12	SOT23-6	Green	Tape & Reel	3000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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