High Efficiency High Voltage 3A Step Down Converter

1 Features

- Input Voltage Range: 4.5V to 25V
- 3A Constant Output Current
- ±1.5% Internal Reference Accuracy Over-Temperature
- Integrated 50mΩ / 40mΩ MOSFETs
- 175μA Quiescent Current
- >90% Efficiency for 12V to 5V/3A or 3.3V/3A Condition
- 500KHz Switching Frequency
- Power Save Mode at Light Load
- Fast Load Transient Response
- Internal Soft Start
- Over-Current Protection(OCP) With Hiccup Mode
- Thermal Shutdown Protection
- Available in an SOT23-6 Package
- RoHS Compliant and Halogen-Free

2 Applications

- Security Cameras
- Flat Panels and Monitors
- Set Top Boxes and Medias Players
- General-Purpose Power Supplies

3 Description

The GD30DC1350 is a high efficiency synchronous step-down switch-mode converter. The device operates from an input voltage from 4.5V up to 25V. The main switch and synchronous switch are integrated in the device with very low R_{DS_ON} and capable of delivering up to 3A current.

The switching frequency is set at 500KHz to minimize output voltage ripple. Fault protections include cycle-by-cycle current limit and thermal shutdown.

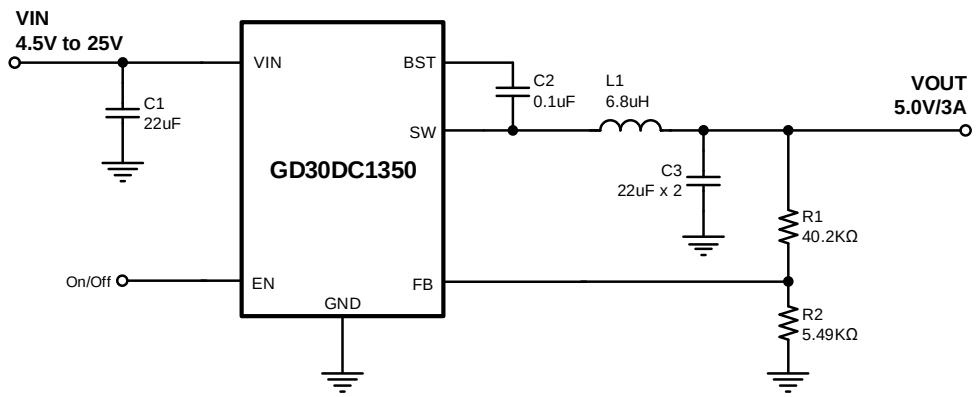
The GD30DC1350 is available with space saving SOT23-6 package and requires minimal number of external components. Together with its low quiescent current, the GD30DC1350 is ideal for security cameras, flat panels and monitors, digital set top boxes etc.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DC1350	SOT23-6	2.92mm x 1.62mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



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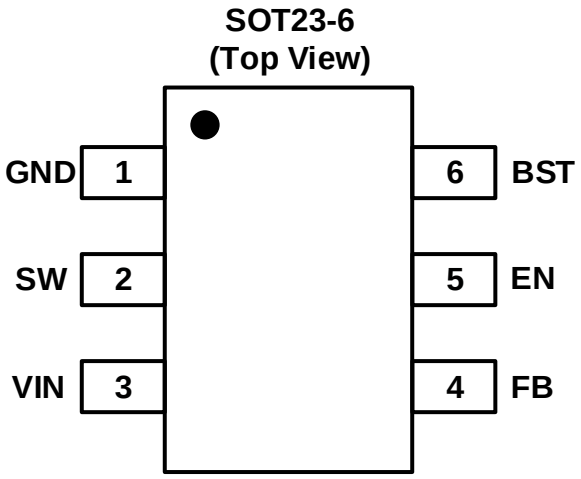
4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	SOT23-6		
GND	1	G	**Power ground**.
SW	2	P	**Switch output**. Connect an inductor to the drains of internal high side NMOS and low side NMOS.
VIN	3	P	**Power supply voltage**. Placed input capacitors as close as possible from VIN to GND to avoid noise influence.
FB	4	I	**Feedback**. Feedback pin for the internal control loop. Connect this pin to the external feedback divider.
EN	5	I	**Enable**. Pull high enables the device, and pull low to disables the device and turns it into shutdown. Don't leave this pin floating.
BST	6	O	**Bootstrap**. A capacitor connection for high-side FET driver. Connect a high-quality, 0.1uF ceramic capacitor from this pin to the SW pin.

1. I = input, O = Output, P = power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Input voltage	−0.3	28	V
V_{SW}	Switching node voltage	−0.3	28	V
V_{BST}	Bootstrap pin voltage	−0.3	32	V
V_{EN}	Enable pin voltage	−0.3	6.5	V
V_{FB}	Feedback pin voltage	−0.3	6	V
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−65	150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.5		25	V
V_{OUT}	Output voltage	0.6		$V_{IN}*D_{MAX}$	V
I_{OUT}	Output current	0		3	A
T_J	Operating junction temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	SOT23-6	117.71	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	SOT23-6	59.55	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	SOT23-6	34.00	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	SOT23-6	59.46	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	SOT23-6	2.27	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 12V, T_J = -40°C to 125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{IN}	VIN operation input voltage		4.5		25	V
V_{UVLO}	Under voltage lockout	V_{IN} falling, V_{EN} = 2V		4		V
V_{UVLO_HYS}	Under voltage lockout hysteresis			330		mV
I_Q	Quiescent current	No switching		175	280	μA
I_{SHDN}	Shutdown current	V_{EN} = 0V		2	10	μA
ENABLE						
V_{EN_RISE}	Rising		1.1	1.2	1.3	V
V_{EN-HYS}	Hysteresis		100	120		mV
I_{EN}	EN input current	V_{EN} = 2V		2	10	μA
VOLTAGE REFERENCE						
V_{FB}	Feedback voltage	T_J = 25°C	588	600	612	mV
I_{FB}	Feedback leakage current	V_{FB} = 0.62V		5	50	nA
INTEGRATED POWER MOSFETS						
$R_{DS(on)}$	High-side FET on resistance	$V_{BST} - V_{SW}$ = 5V		50		mΩ
	Low-side FET on resistance			40		mΩ
SWITCHING REGULATOR						
f_{SW}	Switching frequency	V_{IN} = 12V, Vout = 5V, I_{OUT} = 1.5A T_J = −40°C to 125°C	436	500	580	KHz
t_{ON_MIN}	Minimum on time[2]			95		nS
t_{OFF_MIN}	Minimum off time[2]			220		nS
I_{SW_LKG}	Switch leakage current	V_{EN} = 0V, V_{IN} = V_{SW} = 25V		10	21	μA
CURRENT LIMIT						
I_{LIM_LS}	Low-side valley current limit		3.5	4.7	4.9	A
I_{ZCD}	Zero-Current Detection	V_{IN} = 12V, V_{OUT} = 5V, L = 4.7uH		50		mA

Electrical Characteristics(continued)

V_{IN} = 12V, T_J = -40°C to 125°C, typical value is tested at T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWM						
T_{TSD}	Thermal shutdown temperature[2]		135	150	165	°C
T_{HYS}	Thermal shutdown hysteresis[2]			20		°C

1. Not production tested. Derived by over-temperature correlation.
2. Guaranteed by design and engineering sample characterization.

6 Functional Description

6.1 Block Diagram

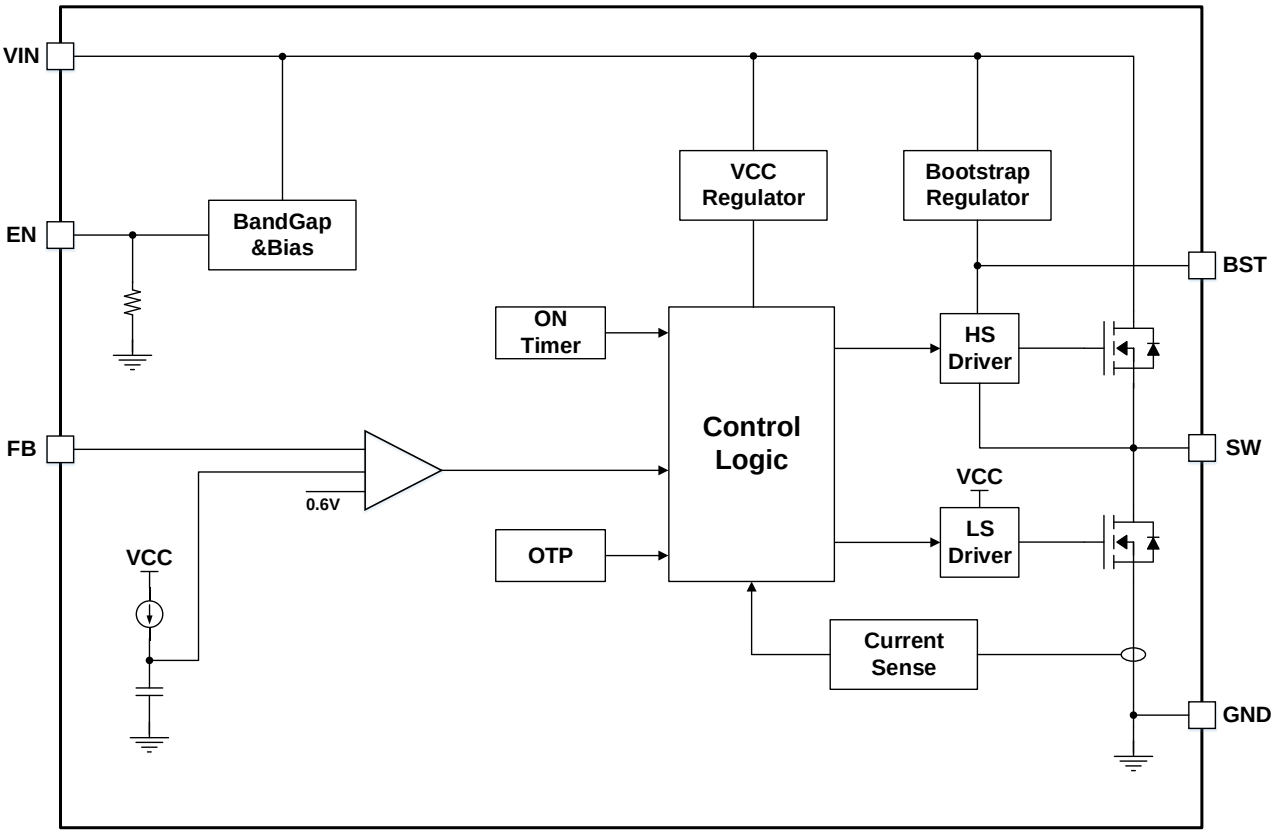


Figure 1. GD30DC1350 Functional Block Diagram

6.2 Operation

The GD30DC1350 is a synchronous switching step-down converter with constant on-time control. The adaptive on-time is so controlled by the input/output voltage that the IC operates at relative constant frequency, typically 500kHz. It is capable of delivering up to 3A for V_{IN} between 4.5V and 25V. The output voltage can be as low as 0.6V.

6.2.1 Constant on-time control

Based on the V_{OUT}/V_{IN} ratio, a simple circuit sets the required on time for the high-side MOSFET. It makes the switching frequency relatively constant regardless of the variation of input voltage, output voltage, and load current. The relation between t_{ON} and V_{IN} and V_{OUT} is defined as following Euqation(1):

$$t_{ON} = \frac{V_{OUT}}{V_{IN}} \times 2us \quad (1)$$

Excellent load transient response is achieved with a unique fast response constant on-time valley current mode. The switching frequency changes during load transition so that the output voltage comes back in regulation faster than a traditional fixed PWM control scheme. Internal loop compensation is integrated which simplifies the design process while minimizing the number of external components.

6.2.2 Pulse Frequency Modulation

The GD30DC1350 automatically operates with pulse frequency modulation (PFM) at light load currents. As the output current decreases, the GD30DC1350 reduces the switching frequency to maintain high efficiency. When the inductor current reaches zero, the low-side MOSFET turns off. Then the output capacitors offer power for load and feedback resistors.

When FB voltage(V_{FB}) drops below the reference voltage, the high-side MOSFET is turned on. As the output current increases, the time period that the current modulator regulates becomes shorter, and the high-side MOSFET turns on more frequently. The switching frequency increases in turn. The output current reaches critical levels when the current modulator time is zero, and can be determined with the following Euqation(2):

$$I_{OUT} = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{2 \times L \times f_{SW} \times V_{IN}} \quad (2)$$

6.2.3 Soft Startup

After enabling the device, internal soft-start circuitry monotonically ramps up the output voltage which reaches nominal output voltage during a soft-start time of 1.5ms (typical). This avoids excessive inrush current and creates a smooth output voltage rise slope.

6.2.4 Pre-Bias startup

The GD30DC1350 is designed for monotonic start-up into pre-biased loads. If the output is pre-biased to a certain voltage during start-up, the BST voltage is refreshed and charged, and the voltage on the soft start is charged as well. If the BST voltage exceeds its rising threshold voltage, and the soft-start voltage exceeds the sensed output voltage at FB, the part works normally.

6.2.5 Bootstrap Charging

An external bootstrap capacitor can supplies the high-side MOSFET driver. This high-side driver has its own UVLO protection. The rising threshold is 2.2V(typical) and a hysteresis is 150mV(typical).V_{IN} regulates the bootstrap capacitor voltage through a diode. The bootstrap regulator maintain a 4.5V(typical) voltage across BST-SW.

6.2.6 Under Voltage Lockout

To avoid mis-operation of the device at an insufficient supply voltage, implement under voltage locking to shutdown the device when the voltage is below the 330mV hysteresis of the 4.0V.

6.2.7 Short Circuit Protection

The GD30DC1350 enters short-circuit protection mode when it reaches the current limit and attempts to recover with hiccup mode. In this process, the GD30DC1350 disables the output power stage, discharges the soft-start capacitor, and then attempts to soft-start again automatically. If the short-circuit condition remains after the soft-start ends, the GD30DC1350 repeats this cycle until the short-circuit disappears and the output rises back to regulation level, the hiccup time typically 6.0ms.

6.2.8 Over Current Protection

The GD30DC1350 has a valley current limit. While the LS-FET is on, the inductor current is monitored. When the

sensed inductor current reaches the valley current limit, the device enters over-current protection (OCP) mode, and the HS-FET does not turn on again until the valley current limit disappears. Meanwhile, the output voltage drops until V_{FB} falls below the feedback under-voltage (UV) threshold. Once the UV condition is triggered, the GD30DC1350 enters hiccup mode (after the SS period) to periodically restart the part. During OCP, the device tries to recover from the over-current fault with hiccup mode. In hiccup mode, the chip disables the output power stage, discharges the soft-start capacitor, and then automatically tries to soft start again. If the over-current condition remains after soft start ends, the device repeats this operation cycle until the over-current conditions disappear. Then the output rises back to the regulation level.

6.2.9 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 150°C(typical), both the high-side and low-side FETs are turned off. Once the device temperature falls below the threshold with hysteresis 20°C (typical), the device returns to normal operation automatically.

6.3 Device Mode Description

6.3.1 Device Enable

When the input voltage is greater than the under-voltage lockout (UVLO) threshold (typically 4.0V), the GD30DC1350 can be enabled by pulling EN higher than 1.2V. Leaving EN floating or pulling it down to ground disables the GD30DC1350. There is an internal 1MΩ resistor from EN to ground.

7 Application Information

The GD30DC1350 device is typically used as a step down converter, which convert an input voltage from 4.5V to 25V to fixed output voltage 5.0V.

7.1 Typical Application Circuit

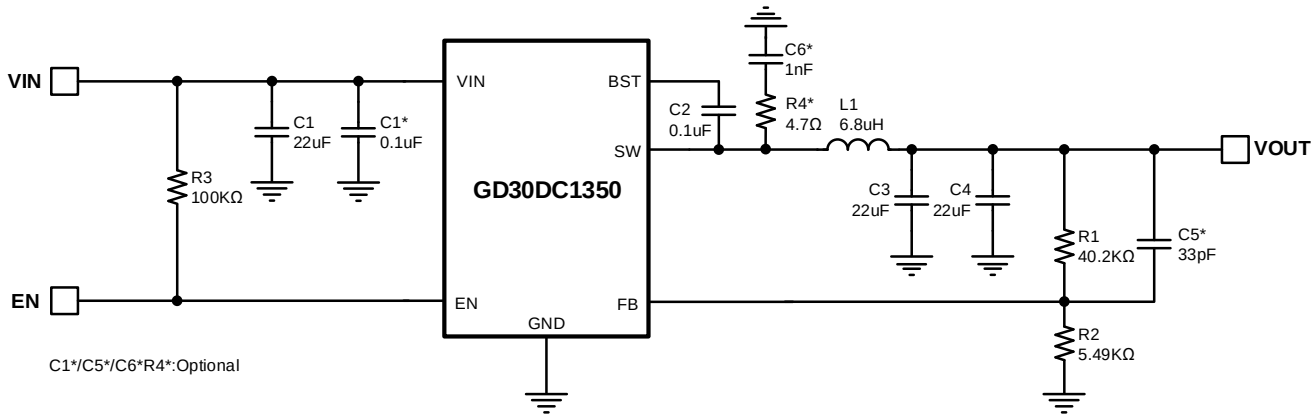


Figure 2. 5.0V, 3A Reference Design

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	4.5V to 25V
Output Voltage	5.0V
Maximum Output Current	3A

Table 2 lists the components used for the example.

Table 2. Design Example Component[1,2]

COMPONENT	DESCRIPTION
C1,C3,C4	22μF, Ceramic Capacitor, 50V, X7R, size 0805
C1*,C2	0.1μF, Ceramic Capacitor, 50V, X7R, size 0603
C5*	Optional, 33pF if it is needed
C6*	Optional, 1nF if it is needed
L1	4.7uH, Power Inductor
R1,R2	Divider resistor, 1%, size 0603
R3	Resistor, 5%, size 0603
R4*	Optional, 4.7Ω if it is needed

1. The components used in these design cases do not belong to GD products, GD does not warrant its accuracy or completeness. GD's customers need to test and verify whether the selected components meet their intended use to ensure stable system operation.
2. Refer to *Detailed Design Description* section for guidance on component selection and calculation equations.

7.3 Detailed Design Description

7.3.1 Output Voltage Setting

An external resistor divider is used to set output voltage according to Equation(3). By selecting R1 and R2, the output voltage is programmed to the desired value. When the output voltage is regulated, the typical voltage reference at the FB pin is 0.6V.

$$V_{OUT} = 0.6V \times \left(1 + \frac{R_1}{R_2}\right) \quad (3)$$

The feedback circuit is shown in Figure 3.

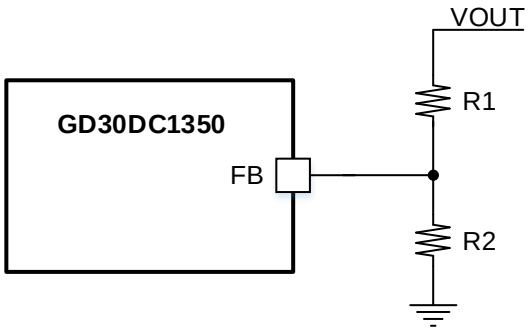


Figure 3. Feedback resistor divider

Table 3 lists the recommended parameters values for common output voltages.

Table 3. Component selection for common output voltages

V_{OUT}(V)	R1(KΩ)	R2(KΩ)	L(μH)
5	90.9	12.4	6.8
3.3	51	11.3	6.8
2.5	51	16.2	4.7
1.8	51	25.5	3.3
1.2	68	68	2.2

7.3.2 Inductor Selection

The inductor selection trade-offs among size, cost, efficiency, and transient response requirements. Three key inductor parameters are specified for operation with the device: inductance value (L), inductor saturation current (ISAT), and DC resistance (DCR). In general, inductors with larger inductance and low DCR values provide much more output and hight conversion efficiency, and smaller inductance values can give batter load transient response.

A good compromise between size and loss is to choose the peak-to-peak ripple current equals to 20% to 40% of the IC rated current. And the peak inductor current can be calculated by Equation(4) and Equation(5). Ensure that the peak inductor current is below the maximum switch current.

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(MAX)} \quad (4)$$

$$I_{L(peak)} = I_{OUT(MAX)} + \frac{\Delta I_L}{2} \quad (5)$$

The switching frequency, input voltage, output voltage, and selected inductor ripple current determines the inductor value according to Equation(6). Once an inductor value is chosen, the peak inductor current is determined by Equation(5). Attention that the inductor should not saturate under the inductor peak current.

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{SW} \times \Delta I_L} \quad (6)$$

7.3.3 Input Capacitor Selection

Input capacitance, C_{IN}, is needed to filter the pulsating current at the drain of the high-side power MOSFET. C_{IN} should be sized to do this without causing a large variation in input voltage. The input capacitance value determines the input voltage ripple of the converter. For most applications, a 22μF capacitor is sufficient.

The peak-to-peak voltage ripple on input capacitor can be estimated with Equation(7):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

For best performance, ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. To compensate the derating of the ceramic capacitors, the voltage rating of capacitor should be twice of the maximum input voltage. The input capacitor also requires an adequate ripple current rating since it absorbs the input switching current.

The input ripple current can be estimated with Equation(8):

$$I_{CIN} = I_{OUT} \times \sqrt{D \times (1-D)} \quad (8)$$

Where D is the duty cycle of converter. The worst-case condition occurs at V_{IN} = 2V_{OUT}. At this point, the input ripple current of input capacitance is equal to half of output current. For simplification, choose an input capacitor with an RMS current rating greater than half of the maximum load current.

7.3.4 Output Capacitor Selection

The output capacitor stabilizes the DC output voltage, it directly affects the steady state, output voltage ripple, loop stability, and output voltage overshoot and undershoot during load current transient.

The output voltage ripple can be estimated with Equation(9):

$$\Delta V_{OUT} = \Delta I_L \times \left(C_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}\right) \quad (9)$$

The output capacitor ripple is essentially composed of two part. One part is caused by the inductor ripple current flowing through the ESR of output capacitors, another part is caused by the inductor ripple current charging and discharging output capacitors. For tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. And when using ceramic capacitors, the capacitance dominates the impedance at the switching frequency and causes most of the output voltage ripple.

The output capacitance must be large enough to supply the current when a large load step occurs. But if the

output capacitor value is too high, the output voltage will not be able to reach the design value during the soft start time. Two 22uF ceramic capacitors are recommended in this application.

7.4 Power Dissipation

For DC-DC, these is still some power deposited on the chip and converted into heat, in spite of switch mode power supplies have considerably higher efficiency when compared to linear regulators. The device power dissipation includes conduction loss, switching loss, gate charge loss and quiescent current losses. The maximum allowable continuous power dissipation at any ambient temperature is calculated by Equation(10):

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}} \quad (10)$$

Where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature and θ_{JA} is the junction to ambient thermal resistance. Once exceeding the maximum allowable power, The device enters thermal shutdown to avoid permanent damage.

8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. For the high-frequency switching converter, a poor layout design can result in poor line or load regulation and stability issues.

1) Place the input/output capacitor and inductor should be placed as close to IC.
2) Keep the power traces as short as possible.
3) The low side of the input and output capacitor must be connected properly to the power GND avoid a GND potential shift.
4) Place the external feedback resistors next to FB.
5) Keep the switching node SW short and away from the feedback network.

For best results, follow the layout example below.

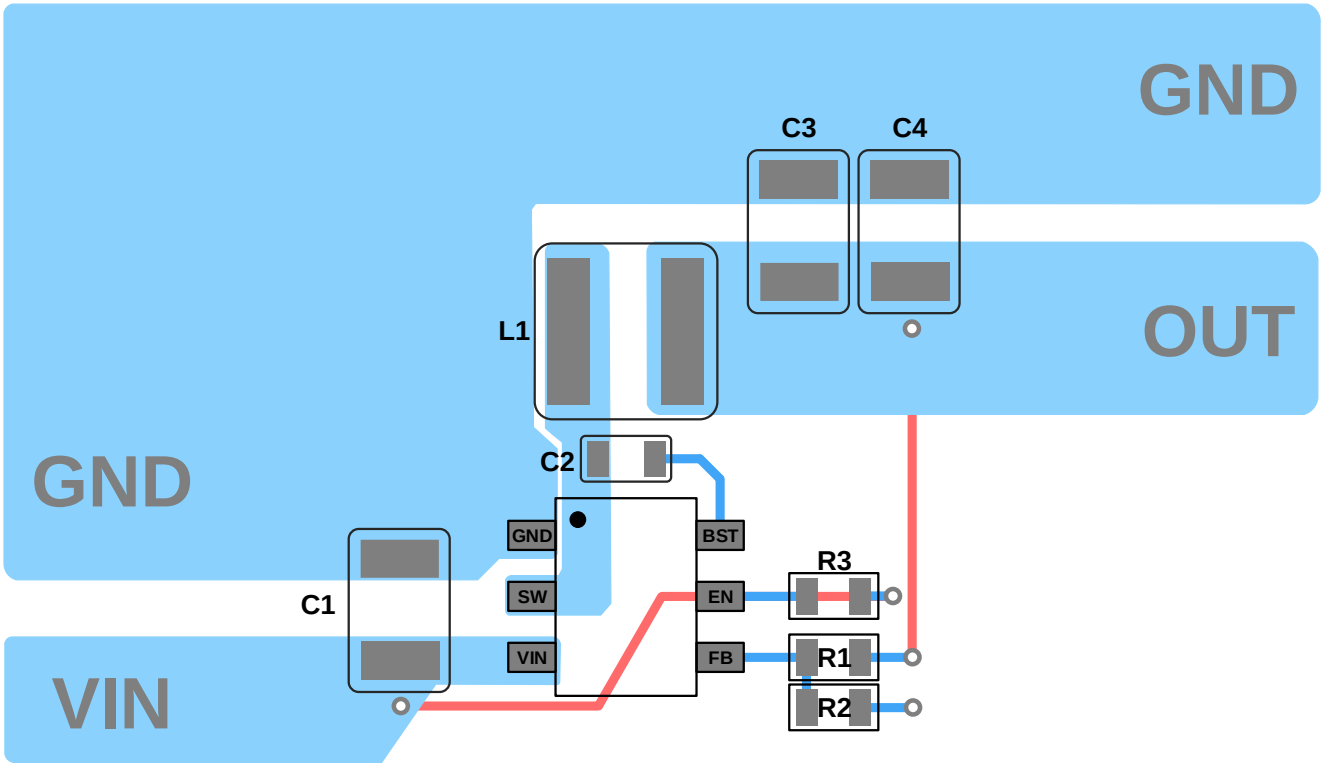
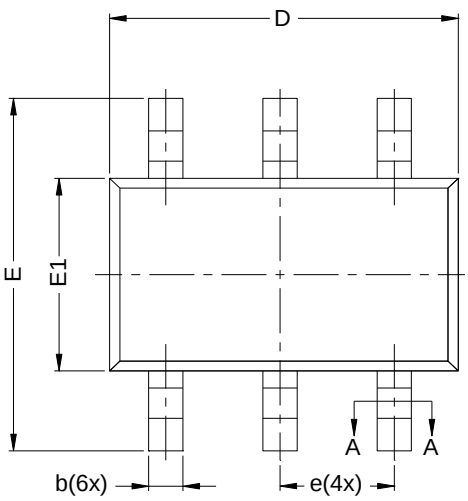


Figure 4. Typical GD30DC1350 Example Layout

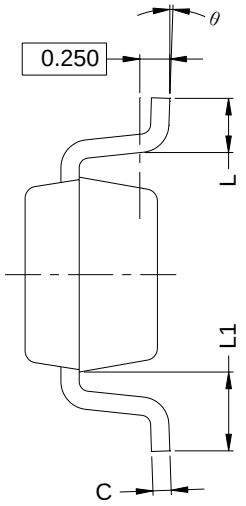
9 Package Information

9.1 Outline Dimensions

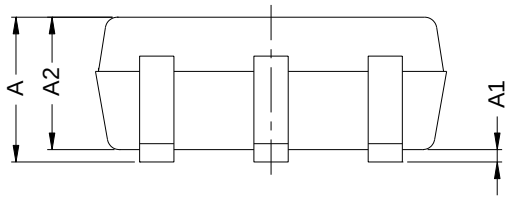
SOT23-6 Package Outline



TOP VIEW



SIDE VIEW



FRONT VIEW

NOTES: (continued)

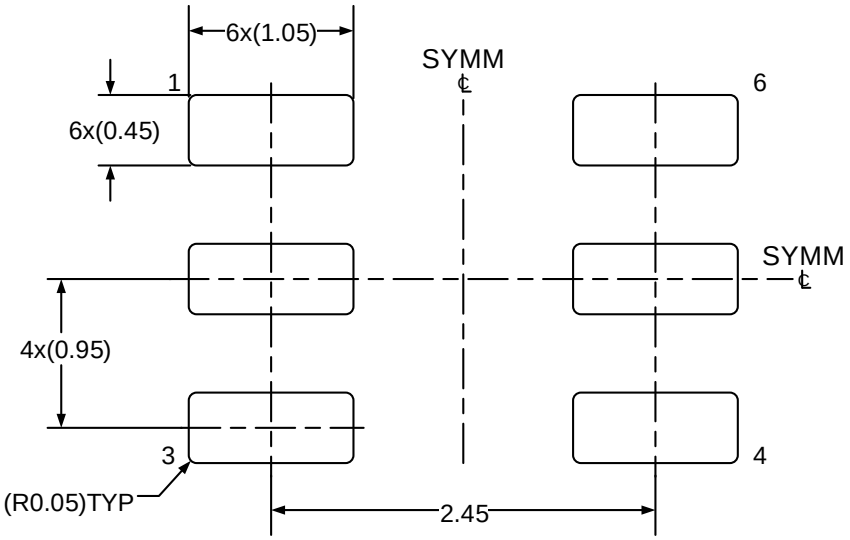
1. Refer to the Table 4 *SOT23-6 dimensions(mm)*.

Table 4. SOT23-6 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A			1.25
A1	0.03	0.08	0.15
A2	1.05	1.10	1.15
b	0.27		0.35
b1	0.26	0.285	0.31
c	0.135		0.23
c1	0.127	0.152	0.178
D	2.82	2.92	3.02
E	2.60	2.90	3.00
E1	1.50	1.62	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.35	0.45	0.55
L1	0.49	0.64	0.79
θ	0°		8°

9.2 Recommended Land Pattern

SOT23-6 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DC1350SSTR-I	SOT23-6	Green	Tape & Reel	3000	−40°C to +85°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024

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