Low-Voltage H-Bridge Driver

1 Features

- H-Bridge Motor Driver
  - Drive a DC Motor or Other Load
  - Low MOSFET ON-Resistance: HS + LS 850mΩ
- 1A Maximum Drive Current
- Separate Motor and Logic-Supply Pins:
  - 0V to 10V Motor Operating Supply Voltage
  - 1.6V to 7V Logic Supply Voltage
- Separate Logic and Motor Power Supply Pins
- Standard PWM Interface (IN1/IN2)
- Low Power Sleep Mode, Maximum Sleep Current 120 nA
  - nSLEEP pin
- Small Package and Footprint
  - 8 pin DFN (With Thermal Pad)
  - 2.00mm x 2.00mm
- Protection Features
  - VCC Undervoltage Lockout (UVLO)
  - Overcurrent Protection (OCP)
  - Thermal Shutdown (TSD)

2 Applications

- Battery-Powered:
  - Cameras
  - DSLR Lenses
  - Consumer Products
  - Toys
  - Robotics
  - Medical Devices

3 Description

The GD30DR3801 provides an integrated motor driver solution for cameras, consumer products, toys, and other low voltage or battery-powered motion control applications. The device has an H-bridge driver, and drives one DC motors, as well as other devices like solenoids. The output driver block consists of N-channel power MOSFETs configured as an H-bridge to drive the motor winding. An internal charge pump generates gate drive voltages.

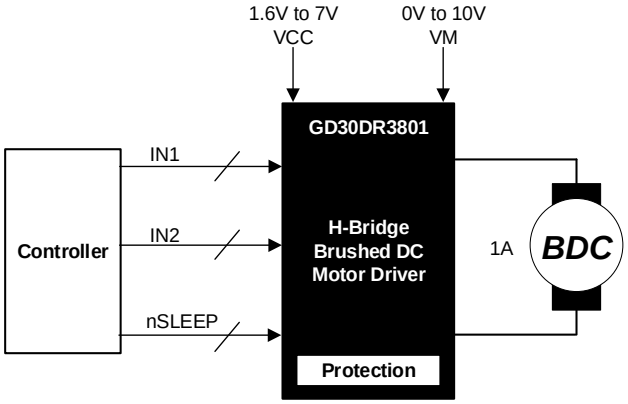
The GD30DR3801 supplies up to 1A of output current. The operates on a motor power supply voltage from 0V to 10V, and control logic can operate on 1.6V to 7V rails.

The GD30DR3801 device has a PWM(IN/IN) input interface. Internal shutdown functions are provided for overcurrent protection, short circuit protection, under-voltage lockout protection, and over-temperature protection.

Device Information[1]

ORDERING CODE	PACKAGE	BODY SIZE (NOM)
GD30DR3801	DFN (8)	2.00 mm × 2.00 mm

1. For packaging details, see *Package Information* section.



Simplified Application Schematic

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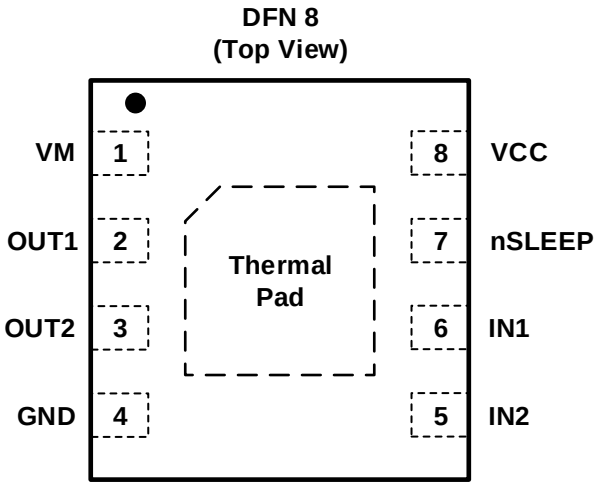
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN		PIN TYPE[1]	FUNCTION
NAME	DFN8		
VM	1	P	Power supply. Connect a 0.1μF bypass capacitor to ground, as well as sufficient bulk capacitance, rated for the VM voltage.
OUT1	2	O	Bridge output 1. Connect to DC motor winding.
OUT2	3	O	Bridge output 2. Connect to DC motor winding.
GND	4	P	Device ground. Connect to board ground.
IN2	5	I	Bridge input 2. Logic high sets OUT2 high. Internal pulldown resistor.
IN1	6	I	Bridge input 1. Logic high sets OUT1 high. Internal pulldown resistor.
nSLEEP	7	I	Sleep mode input. Logic low: the device enters low-power sleep mode. Logic high: the device operates normal mode. Internal pulldown resistor
VCC	8	P	Device supply. Connect a 0.1μF bypass capacitor to ground, rated for the VCC voltage.
Thermal pad	Thermal pad	P	Power ground, connect to board ground, use large ground plane for good thermal dissipation, and multiple nearby vias connecting those planes.(See *Layout Example*).

1. I = input, O = output, P = power, G = ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1,2]

SYMBOL	PARAMETER	MIN	MAX	UNIT
VM	Motor power supply voltage	−0.3	11	V
VCC	Logic power supply voltage	−0.3	7	V
INx, nSLEEP	Control input pin voltage	−0.5	V_{CC}	V
OUTx	Peak motor drive output current	Internally limited		A
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−60	150	°C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to network ground terminal.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
VM	Motor power supply voltage	0		10	V
VCC	Logic power supply voltage	1.6		7.0	V
V_{LOGIC}	Logic level input voltage	0		VCC	V
I_{OUT}	Continuous motor drive output current	0		1.0	A
f_{pwm}	Externally applied PWM frequency	0		250	kHz
T_A	Operating ambient temperature	−40		85	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±4000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±2000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Electrical Characteristics

T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY(VM, VCC)						
VM	VM operating voltage		0		10	V
I_{VM}	VM operating supply current	No PWM, no load		40	100	μA
		50 kHz PWM, no load		0.15	1.0	mA
I_{VMQ}	VM sleep mode supply current	nSLEEP = 0		30	95	nA
I_{VCC}	VCC operating supply current	No PWM, no load		100	200	μA
		50 kHz PWM, no load		0.18	1.0	mA
I_{VCCQ}	VCC sleep mode supply current	nSLEEP = 0		5	25	nA
V_{UVLO}	VCC undervoltage lockout voltage	VCC rising			1.6	V
		VCC falling			1.5	V
LOGIC-LEVEL INPUTS(IN1, IN2, nSLEEP)						
V_{IL}	Input low voltage				$0.25\times V_{CC}$	V
V_{IH}	Input high voltage		$0.5\times V_{CC}$			V
I_{IL}	Input low current	V_{IN} = 0	−5		5	μA
I_{IH}	Input high current	V_{IN} = 3.3V			50	μA
R_{PD}	Pulldown resistance			100		KΩ
H-BRIDGE FETS(OUT1, OUT2)						
$R_{DS(ON)}$	HS+LS FET on resistance	VM = 5V, VCC = 3V, I_O = 800mA, T_J = 25°C		850		mΩ
I_{OFF}	OFF-state leakage current	V_{OUTx} = 0V	−200		200	nA
PROTECTION CIRCUITS						
I_{OFF}	Overcurrent protection trip level		1.2			A
t_{DEG}	Overcurrent de-glitch time			1		μs
t_{OCR}	Overcurrent protection retry time			1		ms
t_{TSD}[1]	Thermal shutdown temperature	Die temperature	150	160	190	°C

1. Not tested in production; based on design and characterization data.

5.5 Timing Requirements

VM = 5V, VCC = 3V, R_L= 20Ω, T_A = 25°C.

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_1	Output enable time		300	ns
t_2	Output disable time		300	ns
t_3	Delay time, INx high to OUTx high		160	ns
t_4	Delay time, INx low to OUTx low		160	ns
t_5	Output rise time		188	ns
t_6	Output fall time		188	ns
t_{wake}	Wake time, nSLEEP rising edge to part active		30	μs

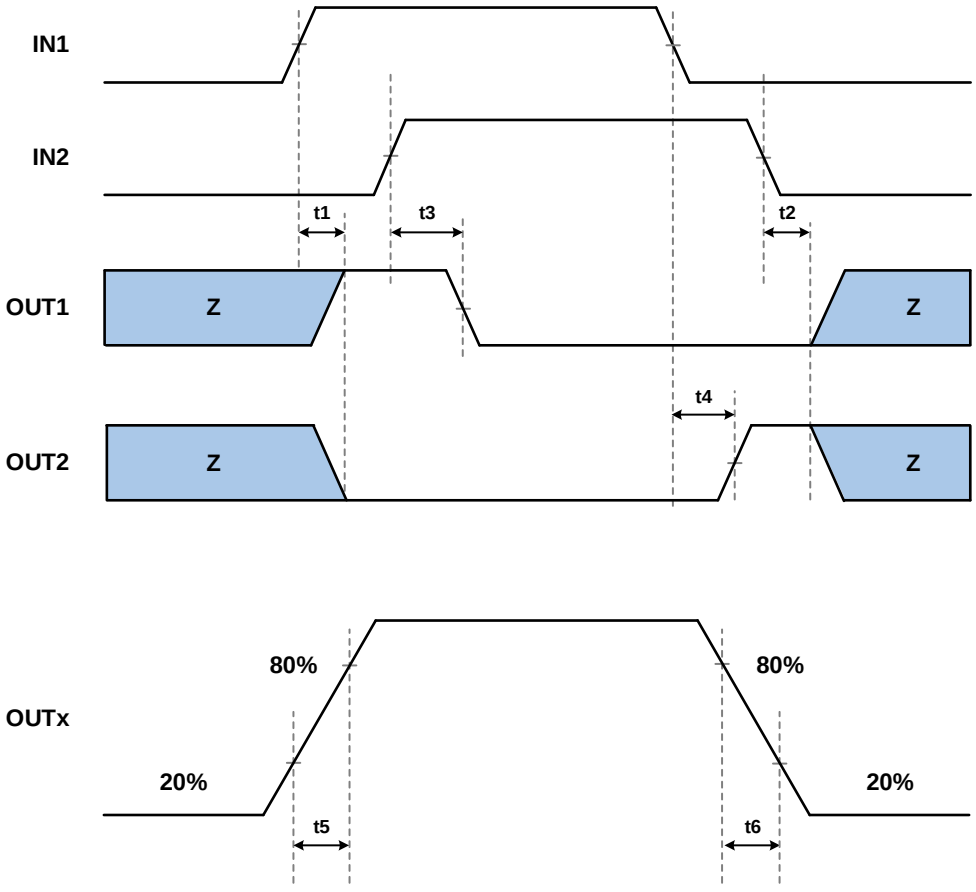


Figure 1. Input and Output Timing for GD30DR3801

6 Functional Description

6.1 Block Diagram

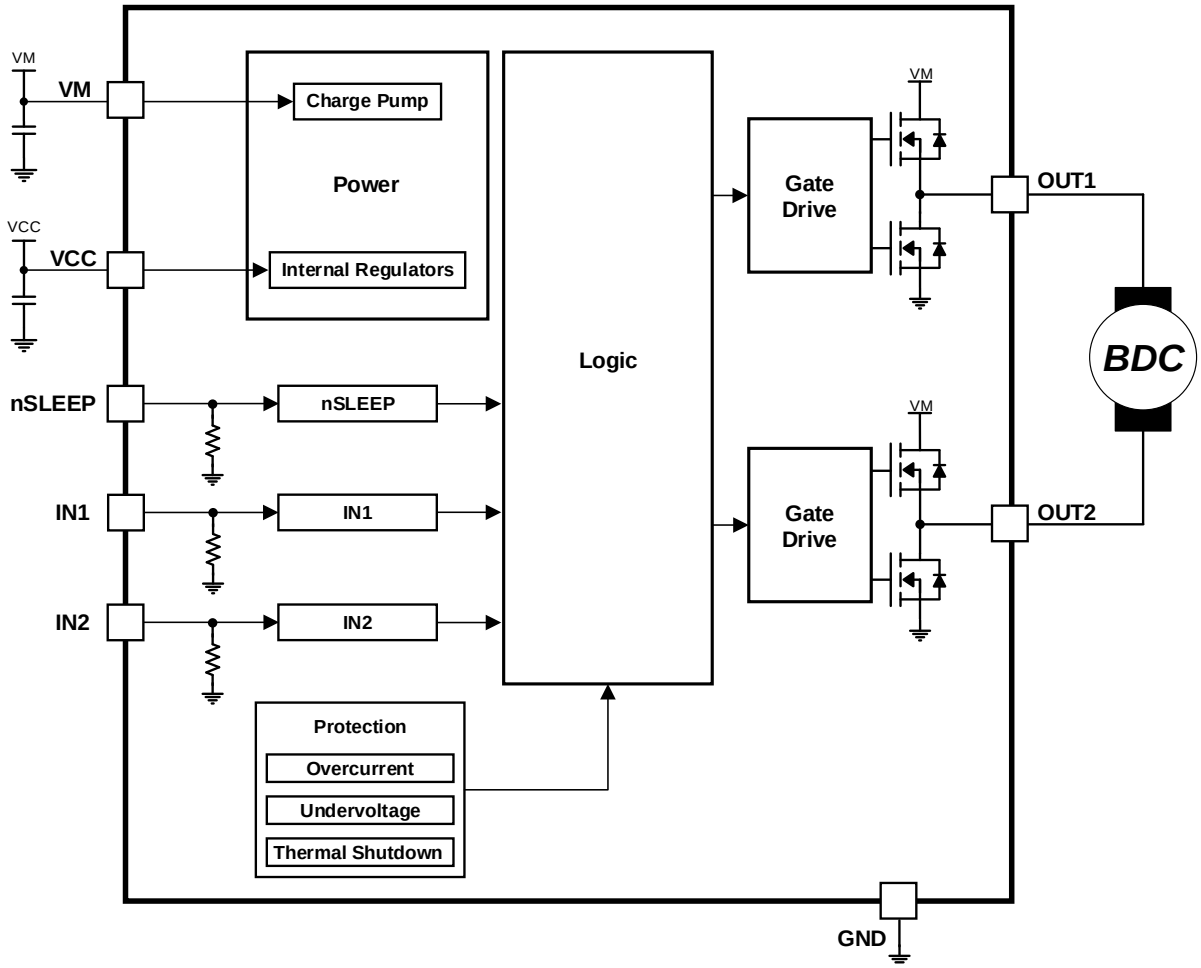


Figure 2. GD30DR3801 Functional Block Diagram

6.2 Operation

The GD30DR3801 serves as an H-bridge driver capable of powering a single DC motor or other devices, such as solenoids. It regulates its outputs through a PWM interface (IN1/IN2) and incorporates a low-power sleep mode, which can be activated via the nSLEEP pin. This device significantly simplifies motor driver systems by integrating the necessary driver FETs and FET control circuitry into a single unit, thus reducing component count. Furthermore, the GD30DR3801 device includes advanced protection features, going beyond traditional discrete implementations, which encompass undervoltage lockout, overcurrent protection, and thermal shutdown.

6.2.1 Bridge Control

The GD30DR3801 utilizes a PWM input interface, which is alternatively referred to as an IN/IN interface. Each input pin corresponds to the control of an individual output.

Table 1 shows the logic for the GD30DR3801 device.

Table 1. H-Bridge Control

nSLEEP	IN1	IN2	OUT1	OUT2	FUNCTION (DC MOTOR)
0	X	X	Z	Z	Coast
1	0	0	Z	Z	Coast
1	0	1	L	H	Reverse
1	1	0	H	L	Forward
1	1	1	L	L	Brake

6.2.2 Sleep Mode

The GD30DR3801 enters a low-power sleep mode when the nSLEEP pin is set to a logic-low state. In this mode, all internal circuitry is powered down.

6.2.3 Power Supplies and Input Pins

The input pins can be driven within the recommended operating conditions with or without the presence of VCC, VM or with both power supplies connected. There is no current leakage path to the power supply. Each input pin includes a weak pulldown resistor (approximately 100 kΩ) connected to the ground.

The VCC and VM supplies can be applied and removed in any order. When the VCC supply is disconnected, the device transitions into a low-power state and expends minimal current from the VM supply. The VCC and VM pins can be connected if the supply voltage is in the range of 1.6V to 7.0V.

The VM voltage supply lacks undervoltage-lockout protection (UVLO). As long as VCC is above 1.6V, the internal device logic remains active. This implies that the VM pin voltage can drop to 0V. However, it's important to note that the load may not be adequately powered at low VM voltages.

6.2.4 Protection Circuits

The GD30DR3801 is equipped with comprehensive protections against VCC undervoltage, overcurrent and overtemperature incidents.

6.2.4.1 VCC undervoltage lockout(UVLO)

If the voltage on the VCC pin drops below the undervoltage lockout threshold at any point, all FETs in the H-bridge are disabled. Normal operation resumes when the voltage on the VCC pin rises above the UVLO threshold.

6.2.4.2 Overcurrent protection (OCP)

Each FET is equipped with an analog current-limit circuit that controls the current by cutting off the gate drive. If this analog current limit persists for a duration exceeding t_{DEG}, all FETs in the H-bridge are disabled. Normal operation automatically resumes after t_{RETRY} has passed. Overcurrent conditions are detected in both the high-side and low-side devices. An overcurrent condition is triggered by a short circuit between the VM pin and GND or between the OUT1 pin and the OUT2 pin.

6.2.4.3 Thermal shutdown (TSD)

If the temperature of the integrated circuit surpasses safe thresholds, all FETs within the H-bridge are disabled. Operation automatically resumes once the temperature returns into a safe range.

Table 2. Fault Conditions Summary

FAULT	CONDITION	H-BRIDGE	INTERNAL CIRCUIT	RECOVERY
VCC undervoltage(UVLO)	V_{CC} < 1.5V	Disabled	Disabled	V_{CC} > 1.6V
Overcurrent(OCP)	I_{OUT} > 1.2A (MIN)	Disabled	Operating	t_{OCR}
Thermal Shutdown(TSD)	T_J > 150°C (MIN)	Disabled	Operating	T_J < 150°C

6.3 Device Modes Description

The GD30DR3801 remains operational unless the nSLEEP pin is set to a logic low state. When in sleep mode, the H-bridge FETs are deactivated and set to a high-impedance state (Hi-Z). The GD30DR3801 device is automatically awakened from sleep mode when the nSLEEP pin is set to a logic high state.

The H-bridge outputs are disabled when undervoltage lockout, overcurrent or overtemperature faults occur.

Table 3. Mode of Operation

OPERATING MODE	CONDITION	H-BRIDGE	INTERNAL CIRCUIT
Operating	nSLEEP high	Operating	Operating
Sleep mode	nSLEEP low	Disabled	Disabled
Fault encountered	Any fault condition met	Disabled	See Table 2

7 Application Information

The GD30DR3801 is typically used to drive one brushed DC motor or other devices like solenoids.

7.1 Typical Application Circuit

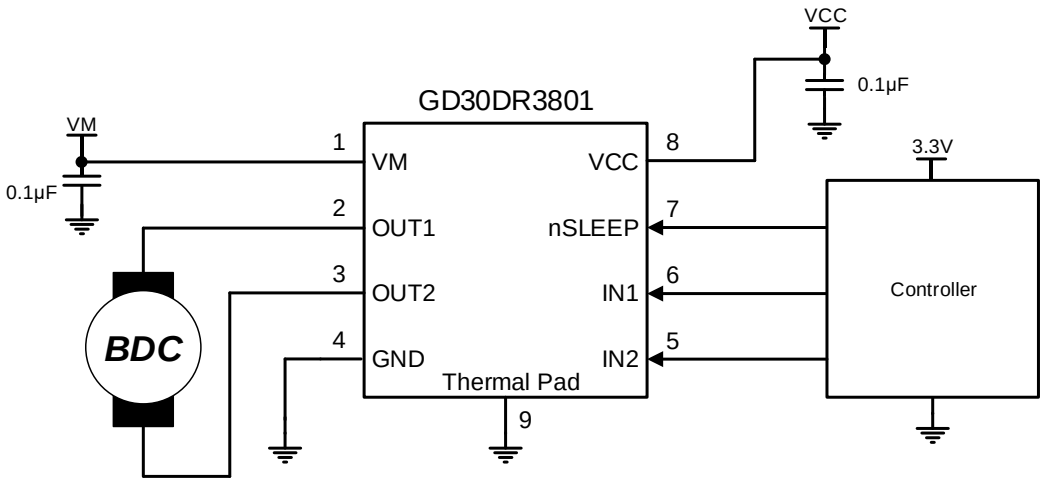


Figure 3. Schematic of GD30DR3801 Application

7.2 Design Example

For this design example, use the parameters in Table 4.

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Motor Supply Voltage	5V
Logic Supply Voltage	3.3V
Target RMS Current	0.5A

7.3 Detailed Design Description

7.3.1 Motor Voltage

The motor voltage to use will depend on the ratings of the motor selected and the desired RPM. A higher voltage spins a brushed DC motor faster with the same PWM duty cycle applied to the power FETs. A higher voltage also increases the rate of current change through the inductive motor windings.

7.3.2 Low Power Mode

When entering sleep mode, GD recommends keeping all input pins low level to minimize system power consumption.

7.4 Power Dissipation

Power dissipation in the GD30DR3801 is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. There is additional power due to PWM switching losses, which are dependent on PWM frequency, rise

and fall time, and VM supply voltages. These switching losses are typically on the order of 10% to 30% of DC power dissipation.

The power dissipation of the GD30DR3801 device is on function of RMS motor current and FET ON-resistance of each output.

$$P_D \approx I_{RMS}^2 \times \left(R_{HS\_DS(ON)} + R_{LS\_DS(ON)}\right) \quad (1)$$

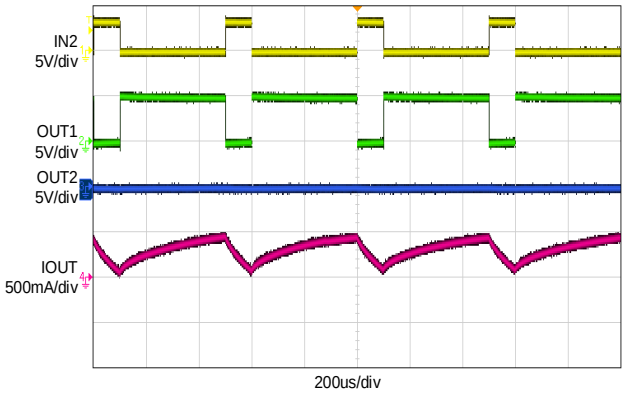
where

- P_D is the device power dissipation
- $R_{HS\_DS(ON)}$ is the resistance of the high-side FET
- $R_{LS\_DS(ON)}$ is the resistance of the low-side FET
- I_{RMS} is the RMS or DC output current being supplied to the load

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

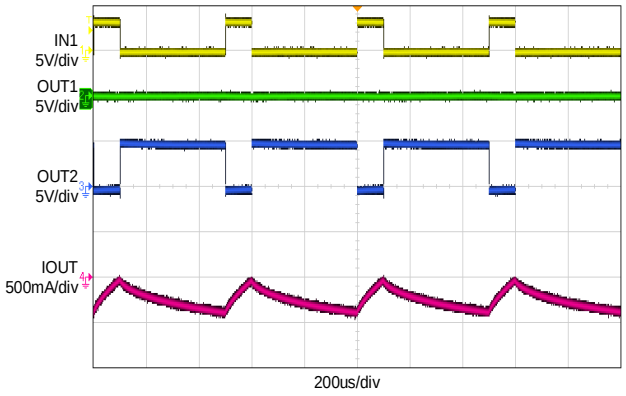
7.5 Typical Application Curves

VM = 5V, VCC = 3.3V, f_{PWM} = 2KHz, T_A = 25°C, unless otherwise noted.



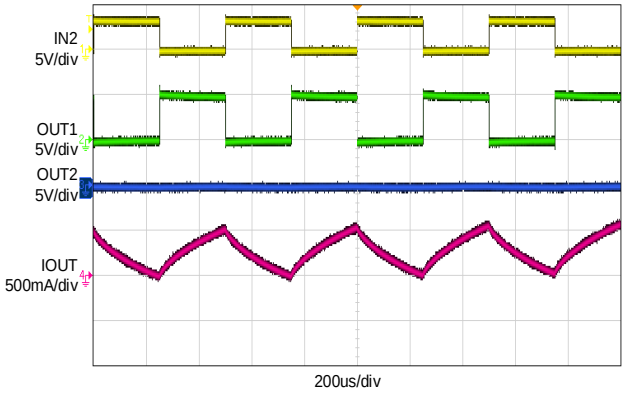
IN1 = 1

Figure 4. 20% Duty Cycle, Forward Direction



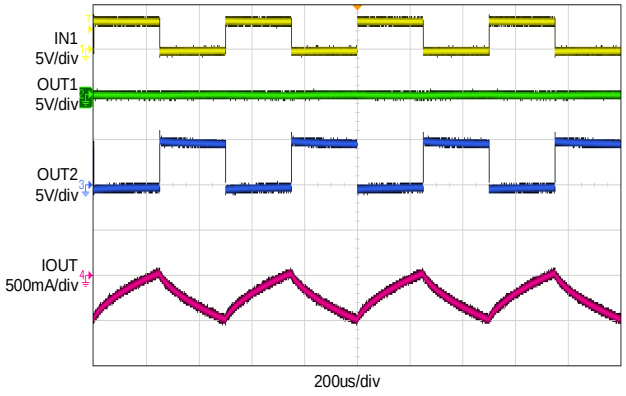
IN2 = 1

Figure 5. 20% Duty Cycle, Reverse Direction



IN1 = 1

Figure 6. 50% Duty Cycle, Forward Direction



IN2 = 1

Figure 7. 50% Duty Cycle, Reverse Direction

8 Layout Guidelines and Example

8.1 Layout Guidelines

Low ESR ceramic capacitors should be utilized for the VM and VCC to GND bypass capacitors. 0.1μF X5R or X7R types are recommended. These capacitors should be placed as close to the VM and VCC pins as possible with a thick trace or ground plane connection to the device GND pin.

In addition, bulk capacitor is required on the VM pin. This bulk capacitor can be ceramic or electrolytic type, but should also be placed as close as possible to the VM pin to minimize the loop inductance.

The high-current device outputs should use wide metal trace, and numerous vias should be used when connecting PCB layers.

8.2 Layout Example

Recommended layout and placement is shown in the following diagram.

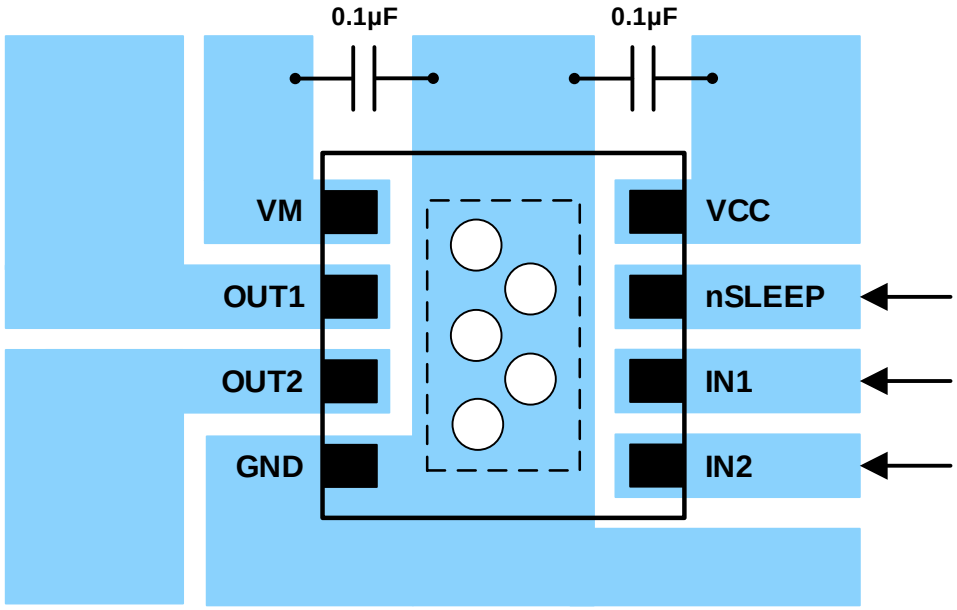
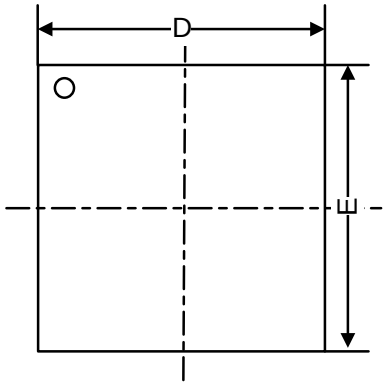


Figure 8. Simplified Layout Example

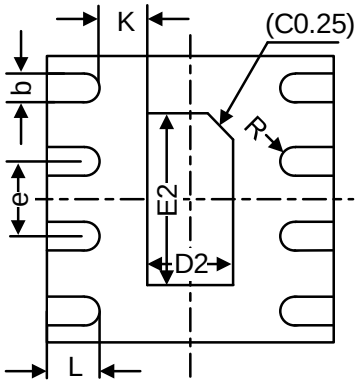
9 Package Information

9.1 Outline Dimensions

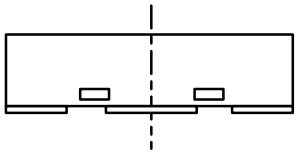
DFN8 Package Outline



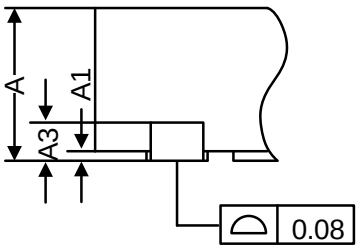
TOP VIEW



BOTTOM VIEW



FRONT VIEW



NOTES:

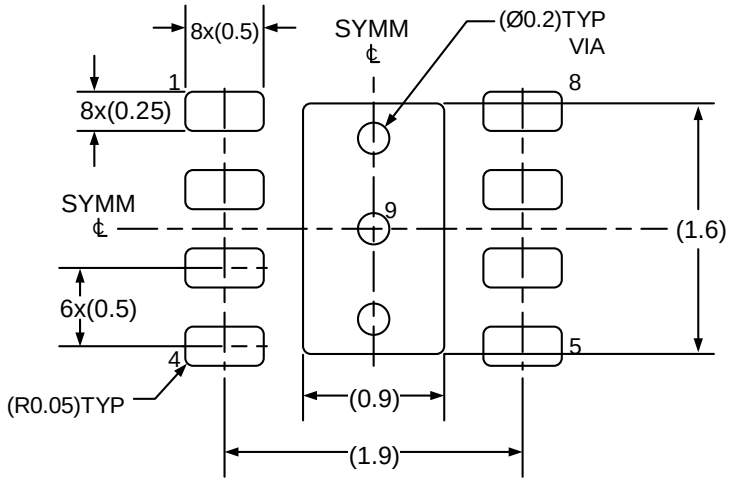
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 5 *DFN8 dimensions(mm)*.

Table 5. DFN8 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
A3		0.20REF	
b	0.15	0.20	0.25
D	1.90	2.00	2.10
E	1.90	2.00	2.10
D2	0.50	0.60	0.70
E2	1.10	1.20	1.30
e	0.40	0.50	0.60
K	0.20		
L	0.30	0.35	0.40
R	0.09		

9.2 Recommended Land Pattern

DFN8 Land Pattern Example



NOTES:

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DR3801WETR-K	DFN8	Green	Tape & Reel	3000	−40°C to +85°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023

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