Low Voltage Multi-Channel Motor Driver

1 Features

- Multi-channel Motor Driver
  - Dual Stepper Motor
  - Single Brushed DC Motor
- Full, Half, 32 Micro-Steps and 64 Micro-Steps
- Built-in DC Motor Driver
  - ±0.5A Maximum Drive Current
- Instruction Cache Function
  - Pre-stores next instruction
- Standard I2C Interface
- Work Status Indication
  - FLAG Pin
- Small Package and Footprint
  - 20 Pin QFN(With Thermal Pad)
- Protection Features
  - Under-voltage Lockout(UVLO)
  - Thermal Shutdown(TSD)

2 Applications

- Robot
- Precision Industrial Equipment
- Camcorder
- Security Camera
- Cradle Head
- Head-shaking Machine

3 Description

The GD30DR4730 is a multi-channel motor driver device that includes two stepper motor drives and one DC motor drive.

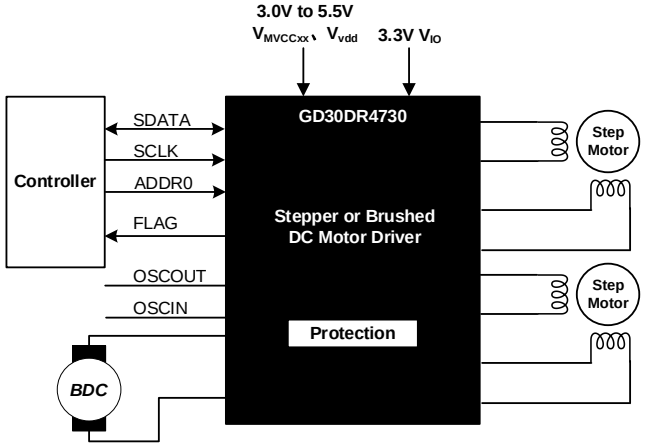
The maximum current of each channel is 0.5A. The device supporting two phase four wires, and four phase five wires stepper motors by I2C communication interface, which is compatible with 1.8V, 2.5V, 3.3V and 5.0V standard industrial interface. The operates on a motor power supply voltage from 3.0V to 5.5V.

Internal shutdown functions are provided for over temperature protection and under-voltage lockout protection.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DR4730	QFN20	3.00 mm × 3.00 mm

1. For packaging details, see *Package Information* section.



Simplified Application Schematic

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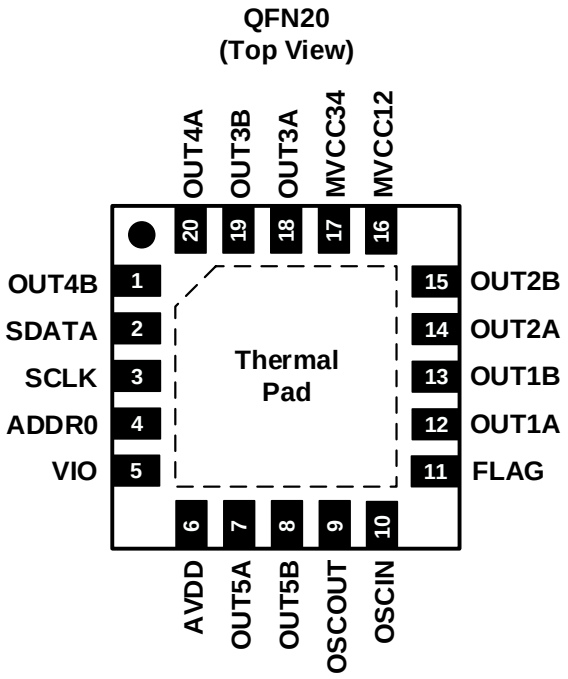
4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN		PIN TYPE[1]	FUNCTION
NAME	NUM		
OUT4B	1	O	Motor output 4B.
SDATA	2	I/O	I2C data line.
SCK	3	I/O	I2C clock line.
ADDR0	4	I/O	I2C address 0.
VIO	5	P	Interface power supply.
AVDD	6	P	Logic power supply for DC motor.
OUT5A	7	O	Motor output 5A.
OUT5B	8	O	Motor output 5B.
OSCOUT	9	O	Reference clock output.
OSCIN	10	I	Reference clock input.
FLAG	11	O	Working Status Flag.
OUT1A	12	O	Motor output 1A.
OUT1B	13	O	Motor output 1B.
OUT2A	14	O	Motor output 2A.
OUT2B	15	O	Motor output 2B.

Pin Description(continued)

PIN		PIN TYPE[1]	FUNCTION
NAME	QFN20		
MVCC12	16	P	Power supply for motor 12.
MVCC34	17	P	Power supply for motor 34.
OUT3A	18	O	Motor output 3A.
OUT3B	19	O	Motor output 3B.
OUT4A	20	O	Motor output 4A.
Thermal Pad	Thermal	G	GND for IC.

1. I = input, O = output, I/O = input/output, P = power, G = ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
VIO	Supply voltage of the interface	−0.3	5.5	V
V_{IN}	Digital input pin voltage[4]	−0.3	VIO+0.3	V
VFLAG	Output Voltage Range	−0.3	6.0	V
MVCCxx	Supply voltage for step motor	−0.3	5.5	V
AVDD	Supply voltage for DC motor	−0.3	5.5	V
IMx(pulse)	Instantaneous H bridge drive current for step motor	−0.6	0.6	A/ch
OUTxA OUTxB	Motor Driver Output Current	−0.5	0.5	A/ch
T_A	Operating ambient temperature[3]	−40	85	°C
T_{stg}	Storage temperature[3]	−55	125	°C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to network ground terminal.
3. Except for the power disspation, operation ambient temperature, and storage temperature, all ratings are for T_A = 25°C.
4. (VIO + 0.3)V must not be exceeded 5.5 V.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
VIO	Supply voltage of the interface	1.8		5.5	V
AVDD	Supply voltage for DC motor	3.3		5.5	V
MVCCxx	Supply voltage for step motor	3.0		5.5	V
I_{OUT}	Continuous motor drive output current	−0.5		0.5	A

1. The device is not guaranteed to function outside of its operating conditions.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±4000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±2000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Electrical Characteristics

MVCC12 = MVCC34 = AVDD = 5.0V, VIO = 3.3V, T_A = 25°C±2°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
V_{VDD}	AVDD and DC Motor supply voltage range		3.0		5.5	V
V_{VIO}	VIO supply voltage range		1.8		5.5	V
V_{MVCCxx}	Step Motor supply voltage range		3.0		5.5	V
$I_{AVDDstandby}$	AVDD supply current on standby	No load		1.2		mA
DIGITAL-LEVEL INPUT & OUTPUT						
V_{IL}	Low-level input		−0.3		$0.31\times V_{IO}$	V
V_{IH}	High-level input		$0.42\times V_{IO}$		$V_{IO}+0.3$	V
f_{CLK}	Input clock		5	27	30	MHz
STEPPER MOTOR DRIVER						
$R_{DS(ON)\_ST}$	HS+LS FET on resistance	I_O = 300mA, T_J = 25°C		1.1		Ω
I_{LEAK_ST}	H bridge leak current	V_{OUTx} = 0V			0.8	μA
DC MOTOR DRIVER						
$R_{DS(ON)\_ST}$	HS+LS FET on resistance	I_O = 200mA, T_J = 25°C		1.4		Ω
I_{LGK_ST}	H bridge leakage current	V_{OUTx} = 0V			0.7	μA
PWM OUT						
V_{FLAG}	Output saturation voltage	I = 5mA			200	mv
I_{LGK_FLAG}	Output leakage current				0.7	μA
PROTECTION CIRCUITS						
T_{TSD}	Thermal shutdown temperature[1]			155		°C
T_{HYS}	Thermal shutdown hysteresis[1]			25		°C
SUPPLY VOLTAGE MONITOR CIRCUIT						
V_{RST_ON}	AVDD Reset operation			2.70		V
V_{RST_HYS}	AVDD Reset hysteresis			0.20		V
V_{ST_ON}	MVCCxx Reset operation			2.70		V
V_{ST_HYS}	MVCCxx Reset hysteresis			0.20		V

1. Not tested in production; based on design and characterization data.

5.5 Timing Requirements

5.5.1 I2C Timing characteristics

T_A = 25℃, VIO = 3.3V, AVDD = 5V, CL = 20 pF(unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{scl}	SCL input cycle				400	kHz
t_{irs}	RST's rising edge to start		500			μs
t_{buf}	Bus idle time during conversion		4.7			μs
t_{hdst}	Initial conditional hold time before the first clock pulse		4.0			μs
t_{low}	Clock low time		4.7			μs
t_{high}	Clock high time		4.0			μs
t_{sust}	Establishment time of repeated start condition		4.7			μs
t_{hdd}	Holding time from falling edge of SCL to SDA (note)		10			ns
t_{sud}	Settling time from SDA to SCL rising edge		250			ns
t_{rc}, t_{rd}	Rising time of SCL and SDA				1000	ns
t_{fc}, t_{fd}	Falling time of SCL and SDA				300	ns
t_{susp}	Establishment time of end condition		4.7			us
t_{ack}	Delay time from falling edge of SCL to response		300		1000	ns

1. The data must be kept for enough time to bridge the transition time t_{fc} on SCL.

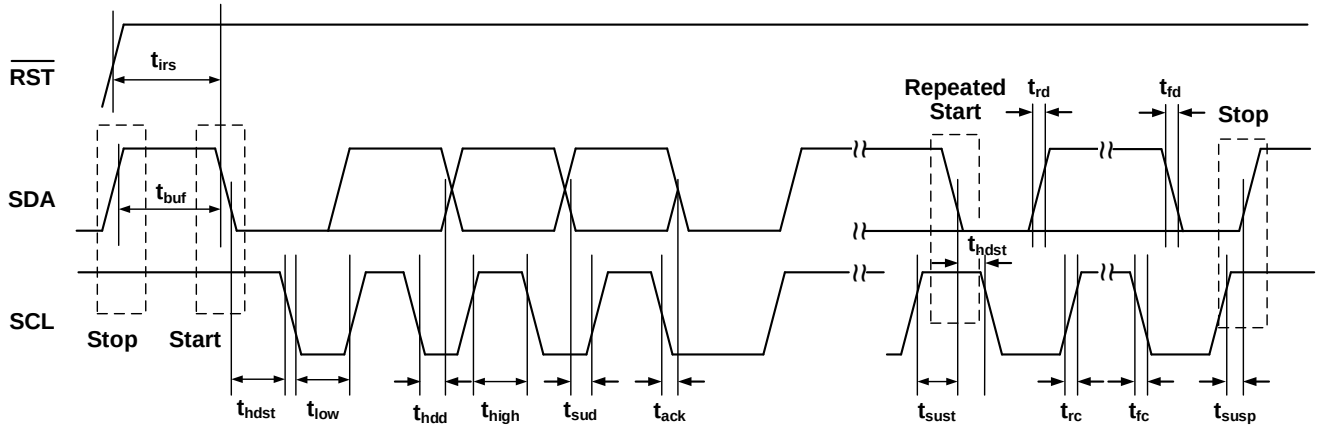


Figure 1. I2C Bus Timing Diagram

5.5.2 Output Timing characteristics

T_A = 25°C, VIO = 3.3V, AVDD = MVCC = 5.0V, and insert 50Ω between output pins(unless otherwise noted).

1CH-5CH: Voltage control type H-bridge.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Tr1	Rising time 1			0.3		μs
Tr2	Rising time 2			0.3		μs
Tf1	Falling time 1			0.03		μs
Tf2	Falling time 2			0.03		μs

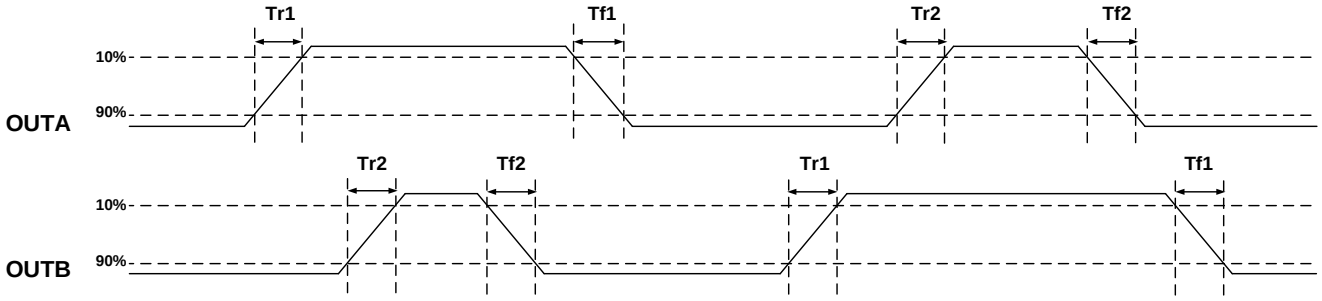


Figure 2. Output Timing Diagram for GD30DR4730

6 Functional Description

6.1 Block Diagram

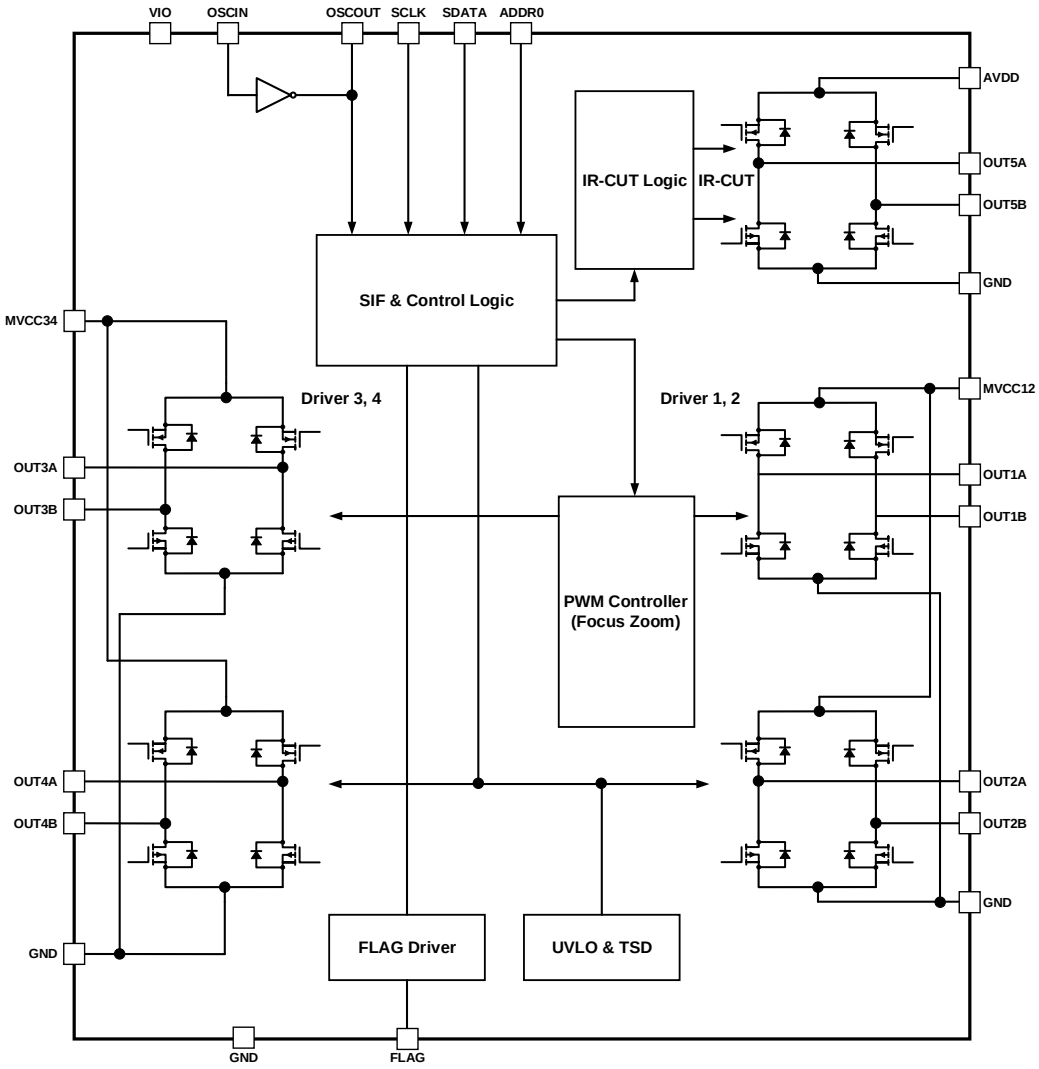


Figure 3. GD30DR4730 Functional Block Diagram

6.2 Operation

The GD30DR4730 is a multi-channel motor driver integrated chip that works under low input voltage with a total of 5 groups of drive output channels. Four groups of motor drive outputs control the X axis and Y axis of the PZT motor with independent quadrature SPWM. Each group of output channels is composed of 4 MOSFETs, and the internal resistance is 1.1Ω. One set of motor drive output ports control IR cut, and conduct internal resistance 1.4Ω. Using I2C control, it is more convenient and accurate to control the motor speed and movement. A variety of protection functions can prevent the equipment against failure occurs.

6.2.1 PZT Control

The GD30DR4730 can control the X-axis and Y-axis of the PZT motor When working in the number of steps

controls the quadrature SPWM mode, also called manual control mode. It can work according to the set target number of turns and phase.

6.2.2 IR-Cut Control

The GD30DR4730 can control IR-Cut at the same time. It can support direction switching at any time. Three working states can be selected: Forward, Reverse and Brake.

6.2.3 VIO Under-voltage Lockout (UVLO)

If at any time the voltage on the VIO pin falls below the under-voltage-lockout threshold voltage, all FETs in the H-bridge will be disabled. Operation resumes when VIO rises above the UVLO threshold.

6.2.4 Thermal Shutdown (TSD)

If the junction temperature exceeds safe limits, all FETs in the H-bridge are disabled. After the junction temperature has fallen to a safe level, operation automatically resume.

6.3 I2C Logic Description

The GD30DR4730 is controlled by I2C communication. SDATA is bidirectional data line, and SCK is clock input. Figure 4 and show the signal timing of a write cycle and a read cycle, respectively. When the clock signal is high, SDATA has a falling edge as the starting condition; When the clock signal is high, the rising edge of SDATA is used as the end condition. All other changes in SDATA occur when the clock signal is low.

In the communication of GD30DR4730, after the initial condition, the first byte (ADDR) consisting of a 7-bit chip address and a 1-bit read/write bit (high for reading and low for writing) is sent to GD30DR4730. The first 3 bits of the 7-bit address are fixed 001, the last 3 bits are fixed 000, the 4th address is controlled by ADDR0 pin, and the 8th bit of the address is read/write. If it is a "write" operation, the next byte contains the register address pointer (MAP), which is used to select the register to be read or written. If it is a "read" operation, the contents of the register pointed by the MAP will be output. MAP is automatically incremented, and the data in the register will appear in turn. Each byte is separated by an acknowledge bit (ACK). GD30DR4730 outputs the reply bit after each input byte reading, and the microcontroller sends the reply bit to GD30DR4730 after each transmitted byte.

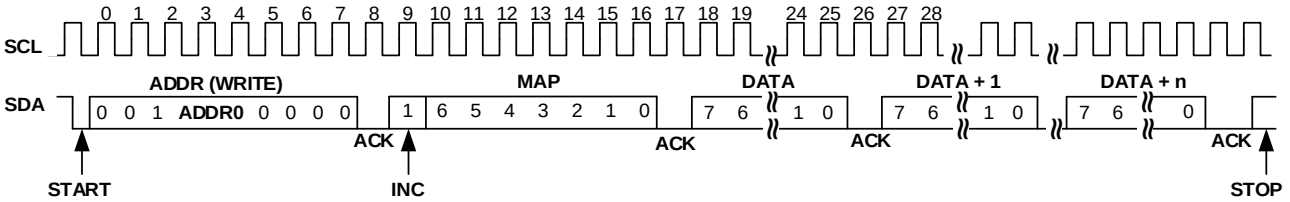


Figure 4. I2C Write Mode

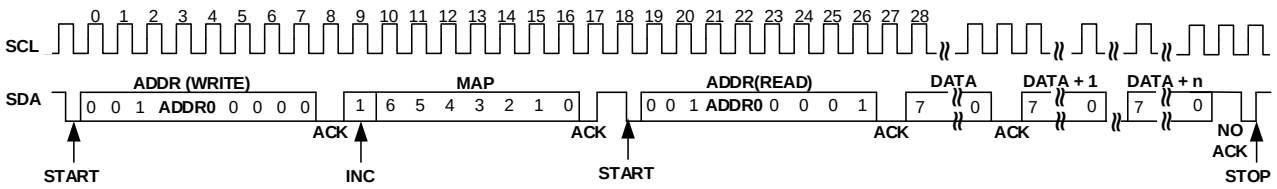


Figure 5. I2C Read Mode

Note that MAP bytes cannot be set during read operations, so a terminated write operation is required as a header

code. As shown in Figure 4, when a stop code is sent as a response to the MAP byte, the write operation is terminated.

Table 1. Register Map

ADDRESS	D7	D6	D5	D4	D3	D2	D1	D0
00H	MOTORSEL	MOTIONPLS	CHIP ID			A_PAUSE	B_PAUSE	CMD_RS
01H	A_CYCLE[7:0]							
02H	A_MODE[1:0]		A_CYCLE[13:8]					
03H	A_PULSE[7:0]							
04H	A_EN	A_RT	A_EXL		A_PULSE[11:8]			
05H	B_CYCLE[7:0]							
06H	B_MODE[1:0]		B_CYCLE[13:8]					
07H	B_PULSE[7:0]							
08H	B_EN	B_RT	B_EXL		B_PULSE[11:8]			
09H	A_START	B_START	A_MS[0]	DC_SRC	DC_CT[1:0]		PWM_CHOP[1:0]	
C0AH	CACHE_PWM	PWM_DUTY[6:0]						
0BH	A_MS[1]	A_BUSY	OTP_ERR	A_WORK	A_STEPS_CU[11:8]			
0CH	A_STEPS_CU[7:0]							
0DH	B_MS[1]	B_BUSY	B_MS[0]	B_WORK	B_STEPS_CU[11:8]			
0EH	B_STEPS_CU[7:0]							
0FH	A_PPW[3:0]				B_PPW[3:0]			

1. In the register table, prefixes A_, B_ and DC_ correspond to A-channel, B-channel and DC motor channel registers respectively.
2. A channel is defined as the output driven by the combination of 1 channel and 2 channels, and B channel is defined as the output driven by the combination of 3 channels and 4 channels.
3. After RESET including power-on reset and reset through CMD_RS register, all registers are set to the initial state, and the default value is 0.
4. For MODE, CYCLE, EN and RT registers, the written data will be valid before the PULSE register is enabled, and will be determined after the address where the PULSE register is located is written. MODE, CYCLE, EN, RT and PULSE registers have cache registers, but other register groups have no cache registers.
5. The data written into the registers of PAUSE, PWM_CHOP, DC_CT and PWM_DUTY will take effect immediately after the data written into their addresses is completed.

Table 2. Register List

ADDRESS	REGISTER NAME/BIT WIDE	FUNCTION
00H	CMD_RS	Resetting registers
	B_PAUSE	B-channel rotation pause
	A_PAUSE	A-channel rotation pause
	CHIP ID	Chip identifier
	MOTIONPLS	Select FLAG port output signal.
	MOTORSEL	Selection of driving mode of stepping motor
01H	A_CYCLE[7:0]	A-channel motor operating frequency
02H	A_CYCLE[13:8]	
	A_MODE[1:0]	A-channel stepping mode
03H	A_PULSE[7:0]	A-channel stepping pulse number
04H	A_PULSE[11:8]	
	A_EXL	A Channel Pre/Post Excitation Time Length
	A_RT	A-channel motor rotation direction
	A_EN	A-channel drive enable
05H	B_CYCLE[7:0]	B-channel motor operating frequency
06H	B_CYCLE[13:8]	
	B_MODE[1:0]	B-channel stepping mode
07H	B_PULSE[7:0]	B-channel stepping pulse number
08H	B_PULSE[11:8]	
	B_EXL	B Channel Pre/Post Excitation Time Length
	B_RT	B-channel motor rotation direction
	B_EN	B-channel drive enable
09H	PWM_CHOP[1:0]	5-channel PWM frequency
	DC_CT[1:0]	5-channel DC motor drive signal
	DC_SRC	5-channel input signal source
	A_MS[0]	A-channel drive mode indication (read-only)
	B_START	B-channel drive start
	A_START	A-channel drive start
0AH	PWM_DUTY[6:0]	5-channel PWM duty cycle setting
	CACHE_PWM	CACHE status indication /PWM signal is output and selected through FLAG port.
0BH	A_WORK	A channel drive status indication (read-only)

ADDRESS	REGISTER NAME/BIT WIDE	FUNCTION
	OTP_ERR	Indication of over-temperature protection function (read-only)
	A_BUSY	A-channel instruction buffer status (read only)
	A_MS[1]	A-channel drive mode indication (read-only)
	A_STEPS_CU[11:8]	Current instruction running steps of channel A (read-only)
0CH	A_STEPS_CU[7:0]	
0DH	B_WORK	B channel drive status indication (read-only)
	B_MS[1:0]	B-channel drive mode indication (read-only)
	B_BUSY	B-channel instruction buffer status (read only)
	B_STEPS_CU[11:8]	Current instruction running steps of channel A (read-only)
0EH	B_STEPS_CU[7:0]	
0FH	B_PPW[3:0]	B-channel PWM maximum duty cycle setting
	A_PPW[3:0]	A-channel PWM maximum duty cycle setting

6.3.1 Configuration register

6.3.1.1 CMD_RS: Resetting register

D0	CONDITION
0	reset (initial condition)
1	releasing reset

1. Resisters are reset to initial condition. You need to set this bit to 1 before you start configuring the other registers.
2. In the initial condition, outputs of constant voltage Driver 1 ~ 5ch are Hi-Z.

6.3.1.2 PAUSE: Force a pause

D2/D1	MOTOR STATE
0	Normal operation (initial state)
1	Stop at the current position immediately

1. After the PAUSE is set to “1” (stop), MODE, CYCLE, RT and EN are kept. After reset to 0, the motor can continue to run according to the original settings. The PULSE register will be cleared, you need to reset the PULSE register.
2. After the PAUSE is set to “1” (stop), you can set EN=0 to clear the number of unfinished steps, and PAUSE=0 to terminate the pause. Reset EN=1, PULSE, CYCLE, and RT parameters, set the corresponding start bit, and the motor will run according to the new parameters.

6.3.1.3 MOTIONPLS: Select the type of FLAG signal

D6	DRIVE TYPE
0	Running status indication
1	Cache register status / PWM output

1. Operation status indication: When a group of instructions of A/B channel run to an end (motor stops), the FLAG pin will output a square wave signal with a pulse width of 128*f_{CLK}, which can be used to inform the main controller that the current motor is in a stopped state.
2. Cache register status PWM output: If CACHE_PWM is set to 1, and A_EN or B_EN is set to 1, the FLAG pin outputs PWM

signals defined by PWM_CHOP and PWM_DUTY; if set to 0, the FLAG pin outputs a PULSE with a width of 128 times the clock width when the values of the pulse and EN cache registers of any channel change from non-zero to zero. If both channels have this change from non-zero value to zero value (at different times), two pulses will be output at corresponding times through the FLAG pin.

3. "f_{CLK}" is the clock frequency of the chip.

6.3.1.4 MOTORSE: Select the motor drive type

D7	DRIVE TYPE
0	2-phase 4-wire motor driver (initial state)
1	4-phase 5-wire motor driver

6.3.1.5 CYCLE: Set the frequency of motor operation

D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	IMPULSE FREQUENCY
00_0000_0000_0000 ~ 00_0000_0000_0111														Disabled (initial state is 0)
0	0	0	0	0	0	0	0	1	0	0	0	0	0	f_{CLK} / (8×4×32)pps
0	0	0	0	0	0	0	0	1	0	0	0	0	1	f_{CLK} / (9×4×32)pps
0	0	0	0	0	0	0	0	1	0	0	0	1	0	f_{CLK} / (10×4×32)pps
~														~
1	1	1	1	1	1	1	1	1	1	1	1	1	0	f_{CLK} / (16382×4×32)pps
1	1	1	1	1	1	1	1	1	1	1	1	1	1	f_{CLK} / (16383×4×32)pps

1. The specified CYCLE is valid for 1-2 phase and 2- phase excitation and micro-step subdivision modes.
2. The initial state only exists after the reset signal is released. If CYCLE is set to a value within the forbidden range (16'b 0000_0000_0000_0000 ~ 16'b 0000_0000_0000_0111), the motor will not operate and you need to make sure the cycle is set in the correct range.
3. f_{CLK} is the clock frequency provided to the main logic.

For example:

input data = 16'b0000_0010_1110_1110, f_{CLK} = 24[MHz]

impulse frequency = 24[MHz]/(750×4×32) =250[pps] =31.25[Hz]

6.3.1.6 MODE[1:0]: Setting of the operation mode

D7	D6	OPERATION MODE
0	0	2-phase excitation| full step (initial condition)
0	1	32 Micro-step
1	0	1-2phase excitation| half step
1	1	64 Micro-step

1. When changing the operation mode, do not set pulse number “0”.
2. At the selection of Micro-step operation, 1-2 phase excitation, 2-phase excitation, the start position varies as shown below:

Table 3. The Selection of Micro-step Operation

BEFORE MODE → AFORE MODE	OPERATION AT THE SELECTION OF MODE
μ step → 1-2 phase	start from the next 1-2phase excitation position to stop position(※1)

BEFORE MODE → AFORE MODE	OPERATION AT THE SELECTION OF MODE
μ step → 2-phase	start from the next 2-phase excitation position to stop position(※2)
32 micro-step → 64 micro-step	start from the stop position
64 micro-step → 32 micro-step	start from the next 32 micro-step position to stop position
1-2 phase → 2-phase	start from the next 2-phase excitation position to stop position(※3)
1-2 phase → μ step	start from the stop position
2-phase → 1-2 phase	start from the stop position
2-phase → μ step	start from the stop position

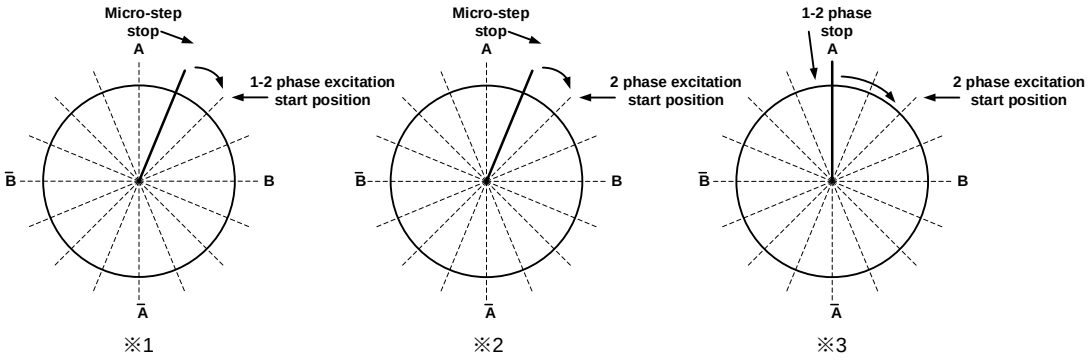


Figure 6. The Selection of Micro-step Operation

When the motor is set to backward rotation direction, it moves to the backward rotation direction.

For ※1, ※2, ※3, the motor moves from the stop position when the stop position is same as the position after the selection of mode.

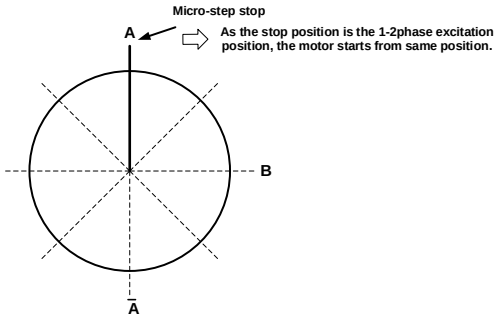


Figure 7. ※1 Example

6.3.1.7 PULSE: Used to make setting of pulse number

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	PULSE NUMBER
0	0	0	0	0	0	0	0	0	0	0	0	0(initial setting)
0	0	0	0	0	0	0	0	0	0	0	1	1 (full step) 1/2 (half step) 1/8 (32 micro-step) 1/16 (64 micro-step)
0	0	0	0	0	0	0	0	0	0	1	0	2 (full step) 1 (half step) 1/4 (32 micro-step) 1/8 (64 micro-step)
~												
0	1	1	1	1	1	1	1	1	1	1	1	2047 (full step) 2047/2 (half step) 2047/8 (32 micro-step) 2047/16 (64 micro-step)
~												
1	1	1	1	1	1	1	1	1	1	1	1	4095 (full step) 4095 (half step upper limit) 4095/8 (32 micro-step) 4095/16 (64 micro-step)

1. step number = Pulse number × Number of driving mode steps.

For example:

A_MODE =“10”(1-2 phase，half step)，PULSE = 12’b0011_1110_1000,

step number = 1000 × 1/2 = 500

A_MODE =“11”(64 micro-step)，PULSE = 12’b0011_1110_1000,

step number = 1000 × 1/16 = 62.5

6.3.1.8 EXL: Set the excitation time of the motor.

D5	EXCITATION TIME
0	0
1	1/2 x Pulse

1. When the excitation time is set to 0, there is no pre-excitation and post-excitation in the stepping channel.
2. When the excitation time is set to 1, the excitation time is 1/2 full step.
3. When EXL is set to 1: When EN changes from 0 to 1, pre-excitation takes effect; When EN changes from 1 to 0, the post excitation takes effect.

6.3.1.9 RT: Setting of the pulse rotating direction

D6	DIRECTION
0	CW (forward rotation, initial setting)
1	CCW (backward rotation)

6.3.1.10 EN: Setting of driver enable control

D7	STATION
0	Hi-Z
1	Normal drive

1. When EN is set to 0, any data written to the PULSE register will be treated as “0”.

6.3.1.11 PWM_CHOP: Setting of PWM chopping frequency

D1	D0	CHOPPING FREQUENCY
0	0	FCHOP = f_{CLK} / 128 (initial setting)
0	1	FCHOP = f_{CLK} / 256
1	0	FCHOP = f_{CLK} / 512
1	1	FCHOP = f_{CLK} / 1024

1. "f_{CLK}" is the clock frequency of the chip.

6.3.1.12 DC_CT: Used to make setting of the statue of the driver

D3	D2	STATUS OF THE DRIVER
0	0	Hi-Z (initial setting)
0	1	Forward rotation
1	0	Backward rotation
1	1	brake

6.3.1.13 DC_SRC: Select the external or internal control

D4	STATE OF THE CONTROL
0	internal control (DC_CT、initial setting)
1	external control

6.3.1.14 START: Enable the A/B channel to start running.

D7/D6	ENABLED STATE
0	None (initial state)
1	A/B channel operation (self-clearing)

1. This register bit is the start pulse of the A/B channel’s running instruction. When it is set to 1, it will be reset to 0 after an SCLK. If the stepping motor is currently running, the instruction loads the settings (PULSE, CYCLE, etc.) into the cache.

6.3.1.15 CACHE_PWM: Setting the FLAG pin output signal mode.

D7	FLAG STATE(MOTIONPLS = 1)
0	The pin directly outputs the state of the buffer register (PULSE, EN), and outputs a pulse with a clock frequency of 128 times when there is a change from a non-zero value to a zero value.
1	When A_EN=1 or B_EN=1, the pin outputs PWM signals defined by PWM_CHOP and PWM_DUTY.

6.3.1.16 PWM_DUTY: Setting PWM duty cycle of DC motor channel

D6	D5	D4	D3	D2	D1	D0	PWM DUTY CYCLE
0	0	0	0	0	0	0	128/128 ×100% (initial setting)
0	0	0	0	0	0	1	1/128 ×100%
~							~
1	1	1	1	1	1	1	127/128 ×100%

1. The duty values are significantly influenced by turn ON or turn OFF time of the output driver, compared to the digital processing accuracy.
2. To avoid that, pay utmost attention to the design of duty values.

6.3.1.17 PPW[3:0]: Set the peak pulse width of stepping driver.

D7/D3	D6/D2	D5/D1	D4/D0	PWM DUTY CYCLE
0	0	0	0	128/128 ×100% (initial setting)
0	0	0	1	1/16 ×100%
~				~
1	1	1	1	15/16 ×100%

6.3.1.18 Cache register

The chip has a built-in cache register that can temporarily register input instructions while the motor is running. After the motor completes the current task, it will continue to run the registered instructions.

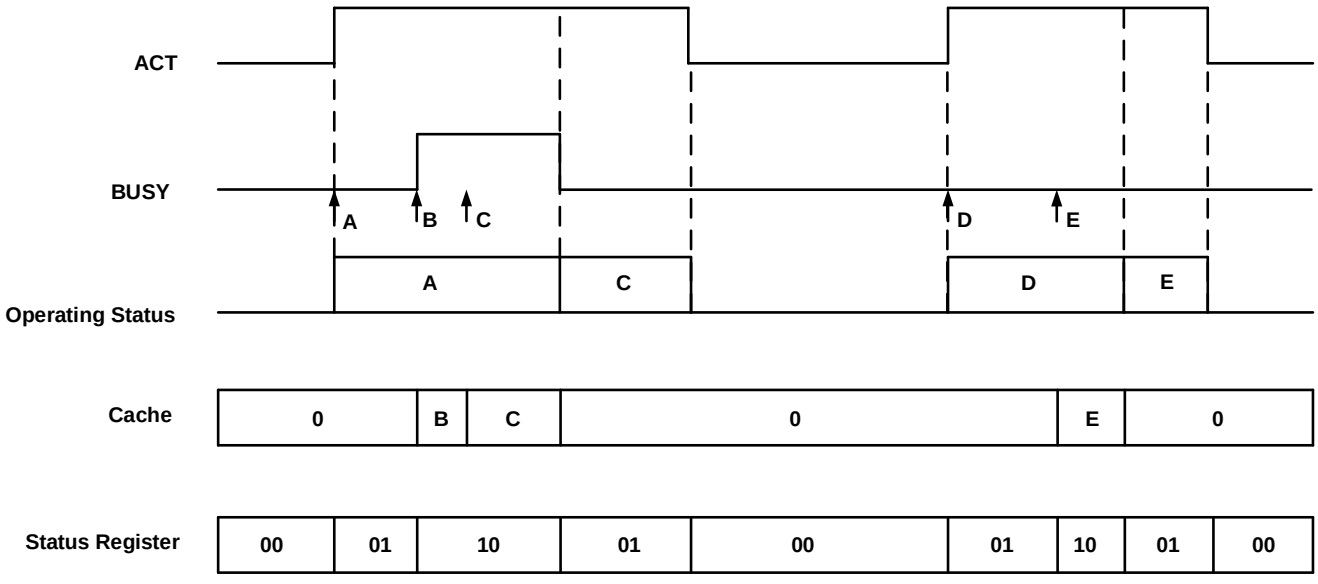


Figure 8. Cache Register

The operation instructions (MODE, CYCLE, RT, PULSE) of the stepping motor are determined after the writing of the address of the PULSE register is completed. When the current instruction runs, the re-entered data will be temporarily stored in the cache register and will be continued after the current instruction is completed. When the data has been registered in the cache, the newly input data can still be received, and the newly input data will overwrite the original data.

The status of the current cache register can be read by both setting MOTIONPLS to 1 and CACHE_PWM to 0.

when the values of PULSE and EN cache registers of any channel change from non-zero values to zero values, the FLAG pin will output a pulse with a width of 128 times the clock width.

If both channels have this change from non-zero value to zero value (at different times), two pulses will be output through the FLAG pin.

6.3.2 Read-only Registers

6.3.2.1 MS: Indicating the current motor drive mode

D7	D5	INDICAING DRIVE MODE
0	0	2 phase | full step(initial setting)
0	1	32 micro-step
1	0	1-2 phase | half step
1	1	64 micro-step

6.3.2.2 BUSY: Indicating the cache register status of the channel.

D5	INDICATING STATUS
0	NO
1	YES

6.3.2.3 OTP_ERR: Indicating the OTP status.

D5	INDICATING STATUS
0	On work
1	In OTP

6.3.2.4 STEP_CU: Indicating the number of integer steps that the current instruction channel has completed.

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	STEP NUMBER
0	0	0	0	0	0	0	0	0	0	0	1	1 (full step) 1/2 (half step) 1/8 (32micro-step) 1/16 (64micro-step)
~												
0	1	1	1	1	1	1	1	1	1	1	1	2047 (full step) 2047/2 (half step) 2047/8 (32micro-step) 2047/16 (64micro-step)
~												
1	1	1	1	1	1	1	1	1	1	1	1	4095 (full step) 4095 (half step) 4095/8 (32micro-step) 4095/16 (64micro-step)

6.3.2.5 WORK: Indicates the motor running state of the channel.

D4	STATE
0	STOP
1	RUN

7 Application Information

The GD30DR4730 is typically used to drive two stepper motors and one brushed DC motor or other devices like solenoids.

7.1 Typical Application Circuit

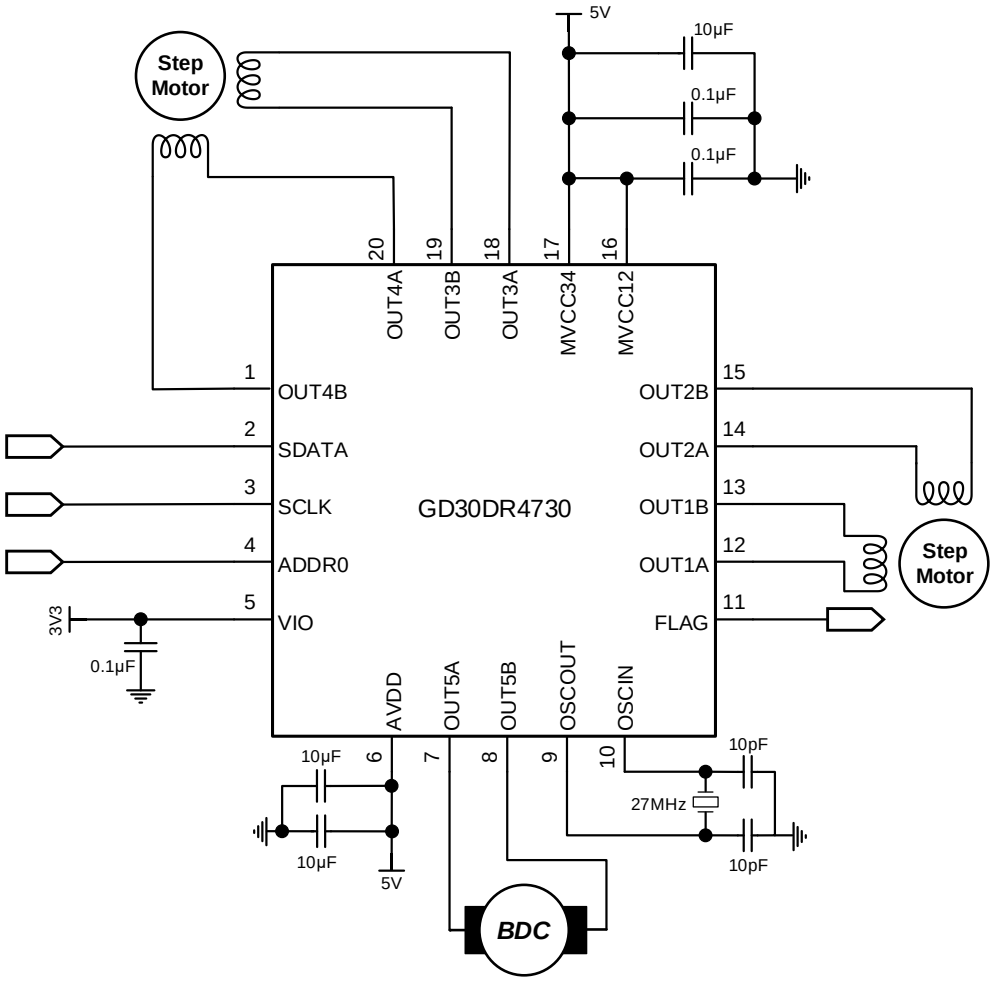


Figure 9. Schematic of GD30DR4730 Application

7.2 Design Example

For this design example, use the parameters in Table 4.

Table 4. Design Parameters

PARAMETER	EXAMPLE VALUE
Motor Supply Voltage	5V
Logic Supply Voltage	3.3V
Target RMS Current	0.5A

7.3 Power Dissipation

Power dissipation in the GD30DR4730 is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. There is additional power due to PWM switcing losses, which are dependent on PWM frequency, rise and fall time, and power supply voltages.

The power dissipation of the GD30DR4730 device is on function of RMS motor current and FET ON-resistance of each ouput.

$$P_D \approx I_{RMS}^2 \times \left(R_{HS\_DS(ON)} + R_{LS\_DS(ON)}\right) \quad (1)$$

where

- P_D is the device power dissipation
- $R_{HS\_DS(ON)}$ is the resistance of the high-side FET
- $R_{LS\_DS(ON)}$ is the resistance of the low-side FET
- I_{RMS} is the RMS or DC output current being supplied to the load

$R_{DS(ON)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

8 Layout Guidelines and Example

Low ESR ceramic capacitors should be utilized for the VIO, AVDD and MVCCxx to GND bypass capacitors. 10uF X5R or X7R types are recommended. These capacitors should be placed as close to the VIO, AVDD and MVCCxx pins as possible with a thick trace or ground plane connection to the device GND pin.

In addition, bulk capacitor is required on the VIO pin. This bulk capacitor can be ceramic or electrolytic type, but should also be placed as close as possible to the VIO pin to minimize the loop inductance.

The high-current device outputs should use wide metal trace, and numerous vias should be used when connecting PCB layers.

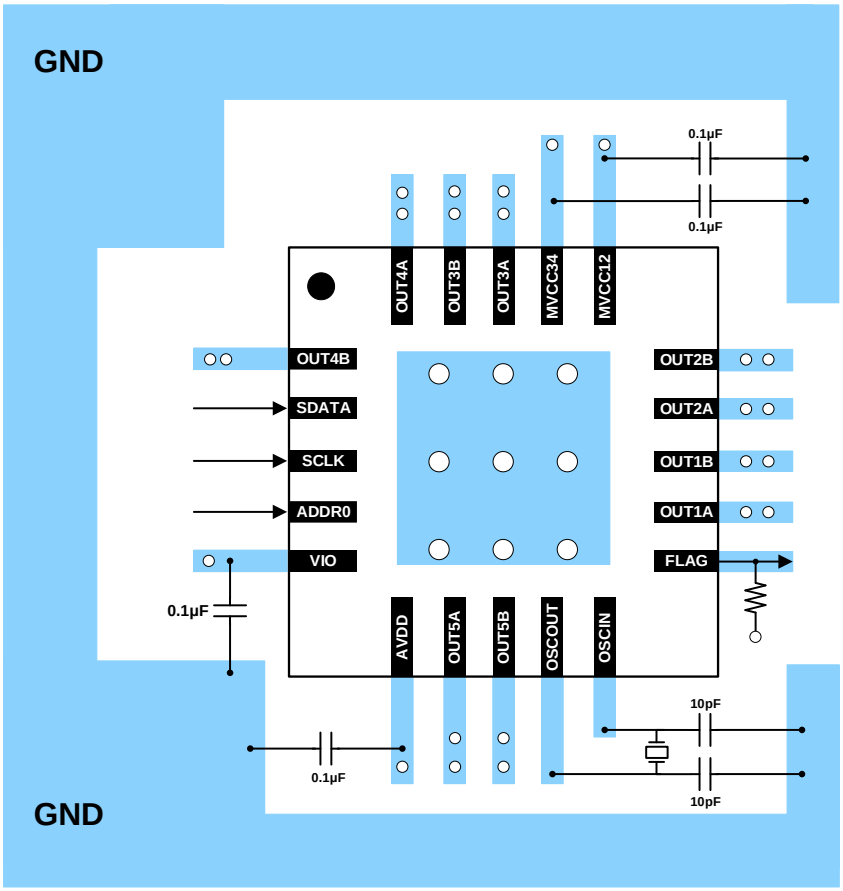
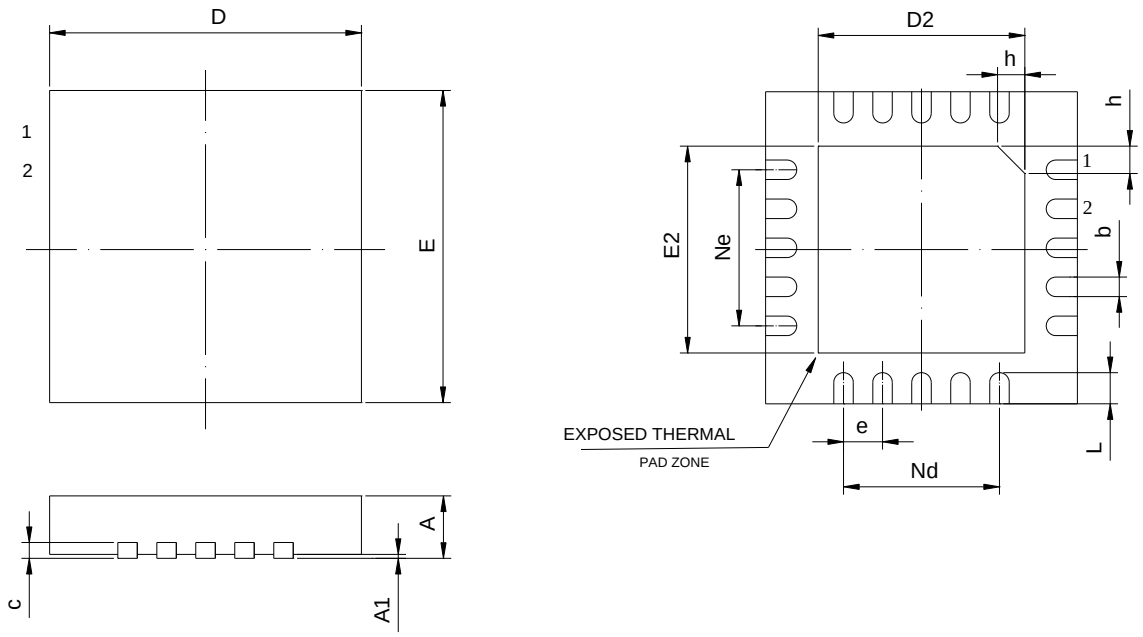


Figure 10. Typical GD30DR4730 Example Layout

9 Package Information

9.1 Outline Dimensions

QFN20 Package Outline



NOTES:

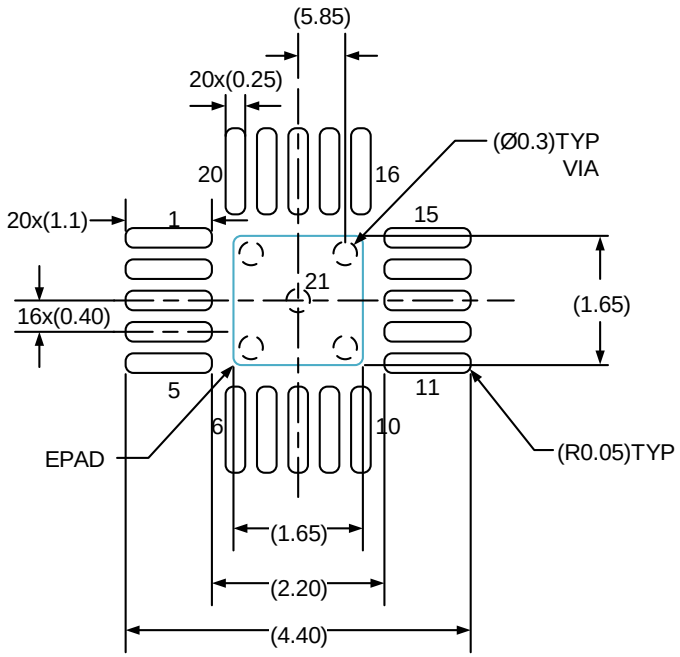
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 5. *QFN20 dimensions(mm)*.

Table 5. QFN20 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
h	0.20	0.25	0.30

9.2 Recommended Land Pattern

QFN20 Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 10X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DR4730FUTR-K	QFN20	Green	Tape & Reel	5000	−40°C to +85°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Preliminary and device details	2023
1.1	1. Modify the 5 *Parameter Information* and 6.3 *I2C Logic Description* contents.	2024

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