Motor Driver IC for Camcorder and Security Camera

1 Features

- Multi-channel Motor Driver
  - Dual Stepper Motor
  - Single Brushed DC Motor
- Up to 1/256-Step Microstepping
- Motor Control by 4-Line Serial Data Communication
- 3.0V to 5.5V Motor Operating Supply Voltage
- Up to 0.5A Output Current
- Work Status Indication
  - LED1 Pin
  - LED2 Pin
- PCB space saving
- Small Package and Footprint
  - 44 pin QFN (With Thermal Pad)
  - 5.00mm x 5.00mm

2 Applications

– IP Cameras, security camera
– Precision Industrial
– Consumer Products
– Robotics

3 Description

The GD30DR4731 provides an integrated motor driver solution for cameras, consumer products, robotics, and other low voltage or battery-powered motion control applications. The device has five H-bridge drivers, of which there are two stepper motor drives and one brushed DC motor drive. The output supports two-phase four-wire and four-phase five-wire stepper motors. The integrated controller enables stepper motor control with microstepping resolution up to 1/256 of a step.

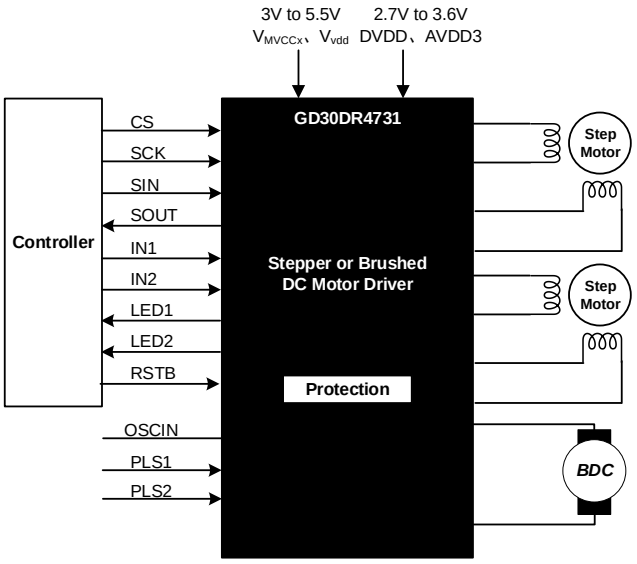
The GD30DR4731 supplies up to 0.5 A of output current. The operates on a motor power supply voltage from 3V to 5.5V.

The GD30DR4731 controls stepper motor through the 4-line serial data communication interface and the brushed DC motor through the PWM(IN1/IN2) interface.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DR4731	QFN44	5.00mm × 5.00mm

1. For packaging details, see *Package Information* section.

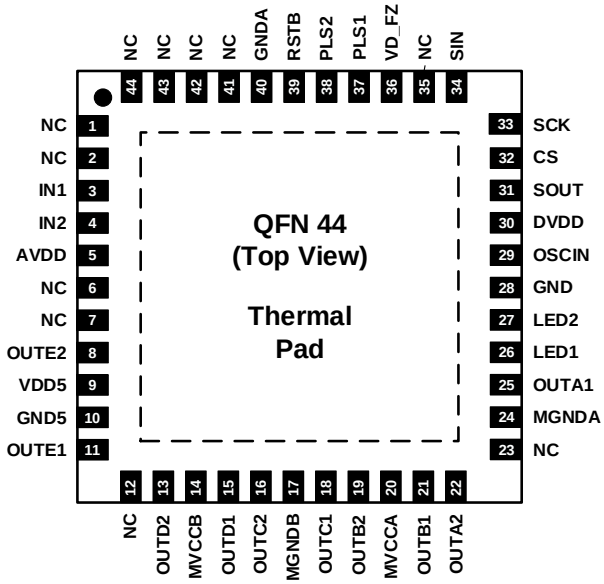


Simplified Application Schematic

Table of Contents

4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN		PIN TYPE[1]	FUNCTION
NAME	QFN44		
NC	1		NC
NC	2		NC
IN1	3	I	Motor IN1 input
IN2	4	I	Motor IN2 input
AVDD	5	P	3 V analog power supply
NC	6		NC
NC	7		NC
OUTE2	8	O	Motor output E2
VDD5	9	P	Power supply for Iris
GND5	10	G	GND for Iris
OUTE1	11	O	Motor output E1
NC	12		NC
OUTD2	13	O	Motor output D2
MVCCB	14	P	Power supply for motor B
OUTD1	15	O	Motor output D1
OUTC2	16	O	Motor output C2
MGNDB	17	G	GND for motor B

PIN		PIN TYPE[1]	FUNCTION
NAME	QFN44		
OUTC1	18	O	Motor output C1
OUTB2	19	O	Motor output B2
MVCCA	20	P	Power supply for motor A
OUTB1	21	O	Motor output B1
OUTA2	22	O	Motor output A2
NC	23		NC
MGNDA	24	G	GND for motor A
OUTA1	25	O	Motor output A1
LED1	26	I	Open-drain 1 for driving LED
LED2	27	I	Open-drain 2 for driving LED
GNDD	28	G	Digital GND
OSCIN	29	I	OSCIN input
DVDD	30	P	3 V digital power supply
SOUT	31	O	Serial data output
CS	32	I	Chip select signal input
SCK	33	I	Serial clock input
SIN	34	I	Serial data input
NC	35		NC
VD_FZ	36	I	Focus zoom sync. signal input
PLS1	37	O	Pulse 1 output
PLS2	38	O	Pulse 2 output
RSTB	39	I	Reset signal input
GNDA	40	G	3V analog GND
NC	41		NC
NC	42		NC
NC	43		NC
NC	44		NC
PGND	Thermal	P	Power ground, connect to board ground

1. I = input, O = output, P = power, G = ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
AVDD3[1]	Controller supply voltage	−0.3		4.0	V
DVDD[1]					
MVCCA[1]	Supply voltage for motor controller 1	−0.3		6.0	V
MVCCB[1]					
VDD5[1]	Supply voltage for motor controller 2	−0.3		6.0	V
Topr[2,4]	Operating ambient temperature	−20		85	°C
Tj[2]	Operating junction temperature	−20		125	°C
Tstg[2]	Storage temperature	−55		125	°C
OUTA1, OUTA2 OUTB1, OUTB2 OUTC1, OUTC2 OUTD1, OUTD2	Motor driver 1 (focus, zoom) H bridge drive current (DC current)	−0.5		+0.5	A/ch
OUTE1, OUTE2	Motor driver 2 (iris) H bridge drive current (DC current)	−0.5		+0.5	A/ch
IM(pulse)	Instantaneous H bridge drive current	−0.6		+0.6	A/ch
Itotal(max)		−0.8		+0.8	A
OSCIN, CS, SCK, SIN, VD_FZ, RSTB[3]	Input Voltage Range	−0.3		DVDD3 + 0.3	V
PLS1, PLS2, SOUT[3]	Output Voltage Range	−0.3		DVDD3 + 0.3	V
LED1, LED2	Output Current Range		30		mA

This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.

When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

1. The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
2. Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.
3. (DVDD + 0.3) V must not be exceeded 4.0 V and (AVDD + 0.3) V must not be exceeded 4.0 V.
4. The power dissipation shown is the value at Ta = 85°C for the independent (unmounted) IC package without a heat sink.

5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
MVCCB, MVCCA	Supply voltage range	3.0	4.8	5.5	V
VDD5[1]		2.7	3.1	3.6	V
DVDD, AVDD3[1]					
VOSCIN, VCS VSCK, VSIN VVD_FZ, VRSTB[2]	Input Voltage Range	−0.3		DVDD + 0.3	V
VPLS1, VPLS2 VSOUT[2]	Output Voltage Range	−0.3		DVDD + 0.3	V
IOUTE2, IOUTE1[1]	Output Current Range	−0.5		+0.5	A
IOUTD2, IOUTD1 IOUTC2 , IOUTC1 IOUTB2 , IOUTB1 IOUTA2, IOUTA1[1]		−0.5		+0.5	A
Ta	Operating ambient temperature	−40		100	°C

1. The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
2. (DVDD + 0.3) V must not be exceeded 4.0 V and (AVDD + 0.3) V must not be exceeded 4.0 V.

5.3 Electrical Characteristics

VDD5 = MVCCx = 4.8V, DVDD = 3.1V, T_A = 25°C ± 2°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT CIRCUIT, COMMON CIRCUIT						
$I_{Omdisable}$	MVCC supply current on Reset	No load, no 27MHz input		0	3.0	uA
$I_{menable}$	MVCC supply current on Enable	Output open		0.5	1.5	mA
$I_{cc3reset}$	3V supply current on Reset	No 27MHz input		0	10.0	uA
$I_{cc3enable}$	3V supply current on Enable	Output open		3.6	20.0	mA
$I_{cc5reset}$	VDD5 supply current on Reset	No 27MHz input		0	3.0	uA
$I_{cc5enable}$	VDD5 supply current on Enable	Output open		0.3	1.0	mA
$I_{ccstandby}$	Supply current on Standby	RSTB = High, output open, 27MHz input, Total current		5.0	10.0	mA
I_{ccps}	Supply current when FZ is Enable	RSTB = High, output open, 27MHz input, FZ = Enable, Total current		6.0	12.0	mA
DIGITAL INPUT / OUTPUT						
$V_{in(H)}$	High-level input	RSTB	0.48 × DVDD		DVDD + 0.3	V
$V_{in(L)}$	Low-level input	RSTB	−0.3		0.2 × DVDD	V
$V_{out(H):SDATA}$	SOUT High-level output	[SOUT] 1mA source	DVDD - 0.5			V
$V_{out(L):SDATA}$	SOUT Low-level output	[SOUT] 1mA Sink			0.5	V
$V_{out(H):MUX}$	PLS1 to 2 High-level output		0.9×VDD			V
$V_{out(L):MUX}$	PLS1 to 2 Low-level output				0.1 × VDD	V
$R_{pullret}$	Input pull-down resistance	RSTB	50	100	200	KΩ
MOTOR DRIVER 1(FOCUS, ZOOM)						
R_{onFZ}	H bridge ON resistance	IM = 100mA	0.6	0.8	1.4	Ω
I_{leakFZ}	H bridge leak current				0.8	uA
LED DRIVER						
R_{onLED}	Output ON resistance	I = 20mA, 5V cell		15	20	Ω
I_{leakIR}	Output leak current				0.8	uA
MOTOR DRIVER 2(IR - CUT) VDD5 = 5V, RL = 20Ω, TA = 25°C						
R_{oncut}	H bridge ON resistance	IM = 300mA		20	2.5	Ω
$I_{leakcut}$	H bridge leak current				0.8	uA
t_r	Rise time		30		188	ns
t_f	Fall time		30		188	ns

Electrical Characteristics(continued)

VDD5 = MVCCx = 4.8V, DVDD = AVDD = 3.1V, T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_d	Delay time from SPI in to OUTE on			25 × T_{SCK}		s
SERIAL PORT INPUT[1]						
Sclock	Serial clock		1		5	MHz
T1	SCK low time		100			ns
T2	SCK high time		100			ns
T3	CS setup time		60			ns
T4	CS hold time		60			ns
T5	CS disable high time		100			ns
T6	SIN setup time		50			ns
T7	SIN hold time		50			ns
T8	SOUT delay time				60	ns
T9	SOUT hold time		60			ns
T10	SOUT Enable-Hi-Z time				60	ns
T11	SOUT Hi-Z-Enable time				60	ns
T_{SC}	SOUT C load				40	pF
DIGITAL INPUT/OUTPUT[1]						
V_{INH}	High-level input threshold voltage	SCK, SIN, CS, VD_FZ		1.36		V
V_{INL}	Low-level input threshold voltage	SCK, SIN, CS, VD_FZ		1.02		V
V_{hysin}	Input hysteresis width	SCK, SIN, CS, VD_FZ		0.34		V
V_{OSC}	OSCIN DC voltage	OSCIN floating		1.3		V
V_{OSCDC}	OSCIN DC input coupling voltage		1.4			V
V_{OSCAC}	OSCIN AC input coupling voltage	C_{COUP} = 0.1μF	1.3			V
T_{rst}	RSTB signal pulse width		100			us
VD_W	Video sync. Signal width		80			us
$T_{(VD-CS)}$	CS signal wait time 1		400			ns
$T_{(CS-DT1)}$	CS signal wait time 2		5			us
PULSE GENERATOR[1]						
$PL1_{wait}$	Pulse start resolution for pulse 1	OSCIN = 27MHz		20.1		us
$PL1_{width}$	Pulse resolution for pulse 1	OSCIN = 27MHz		1.20		us
$PL2_{wait}$	Pulse start resolution for pulse 2	OSCIN = 27MHz		20.1		us
THERMAL SHUTDOWN[1]						
T_{tsd}	Thermal shutdown temperature			145		°C
T_{hys}	Thermal shutdown hysteresis			35		°C
SUPPLY VOLTAGE MONITOR CIRCUIT[1]						
V_{rston}	3.3 V Reset operation			2.48		V

Electrical Characteristics(continued)

VDD5 = MVCCx = 4.8V, DVDD = AVDD = 3.1V, T_A = 25°C (unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{rsthys}	3.3 V Reset hysteresis			0.20		V
$V_{rstFZon}$	MVCCB Reset operation			2.42		V
$V_{rstFZhys}$	MVCCB Reset hysteresis			0.21		V
$V_{rstlSon}$	VDD5 Reset operation			2.42		V
$V_{rstlShys}$	VDD5 Reset hysteresis			0.21		V

1. Guaranteed by design.

6 Functional Description

6.1 Block Diagram

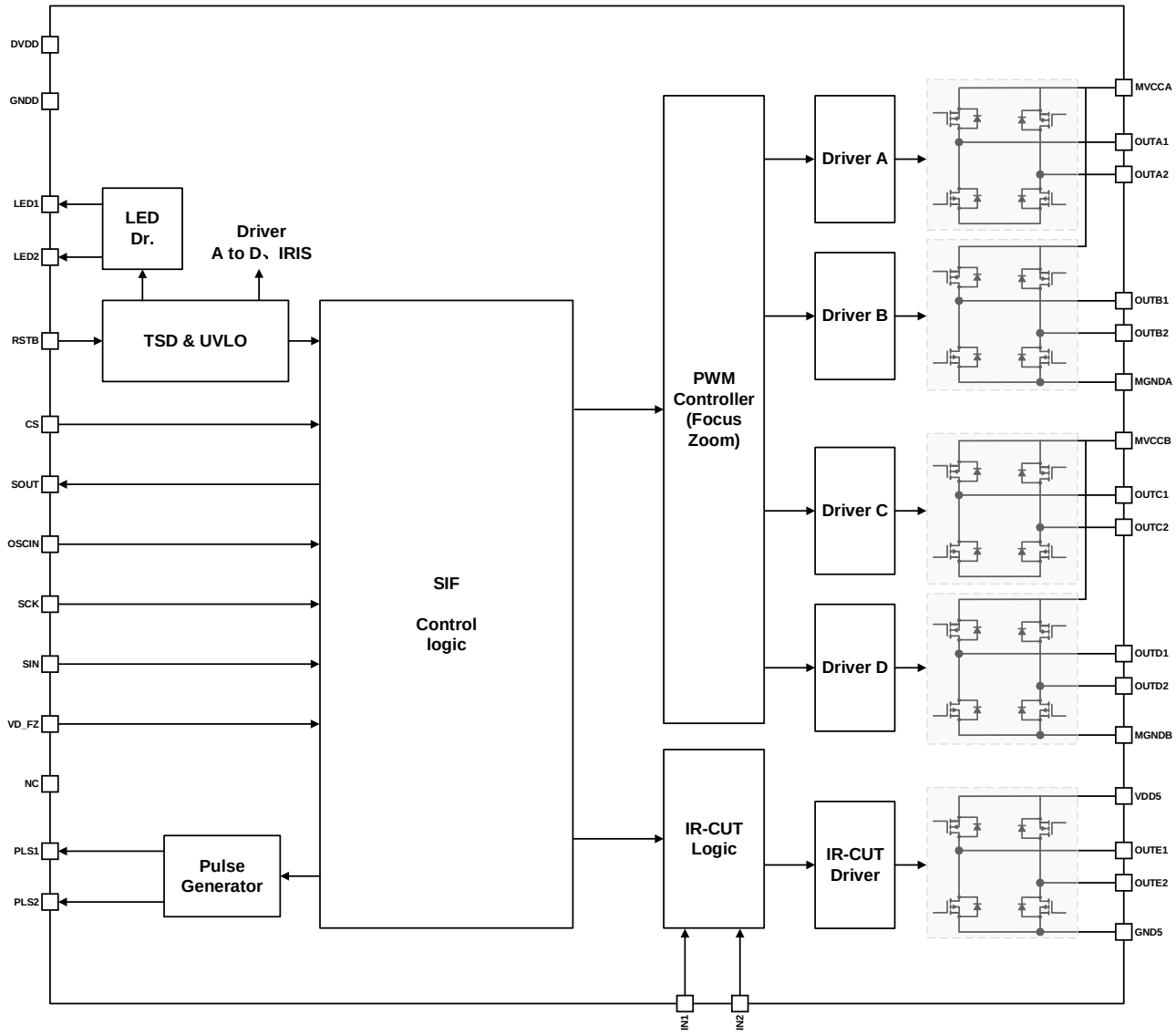


Figure 1. GD30DR4731 Functional Block Diagram[1]

1. This block diagram is for explaining functions. The part of the block diagram may be omitted, or it may be simplified.

6.2 Serial Interface

6.2.1 Timing Chart

The characteristics listed below are reference values derived from the design of the IC and are not guaranteed.

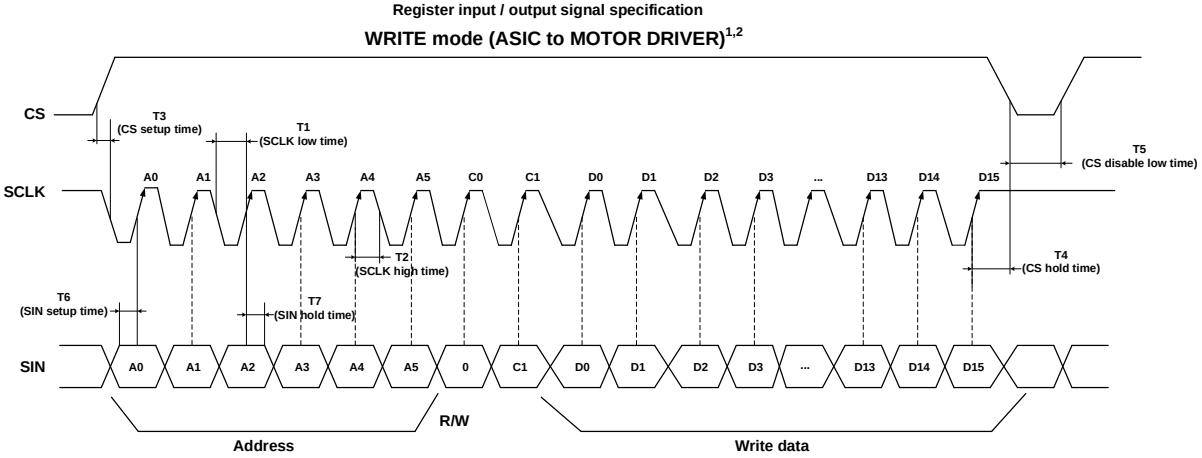


Figure 2. Write Mode Timing

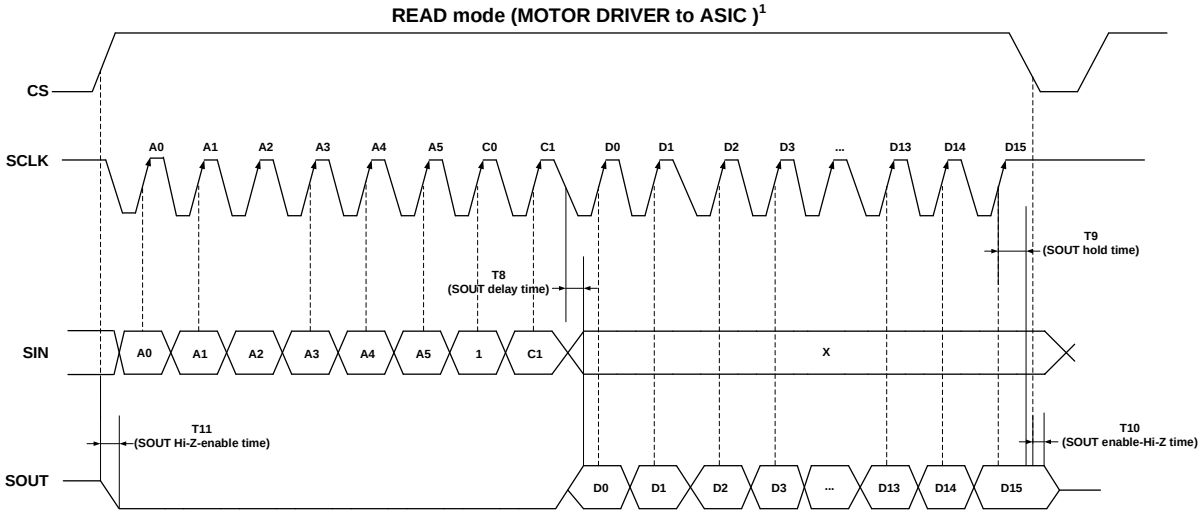
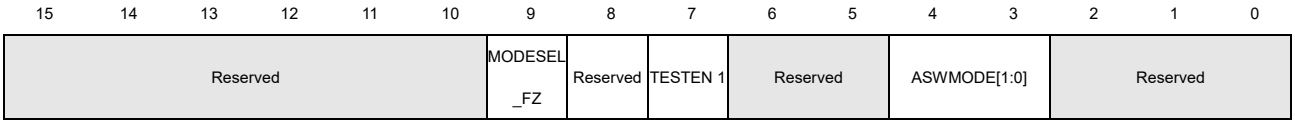


Figure 3. Read Mode Timing

1. CS default value of each cycle (Write / Read mode) starts from Low-level.
2. It is necessary to input the system clock OSCIN at write mode.

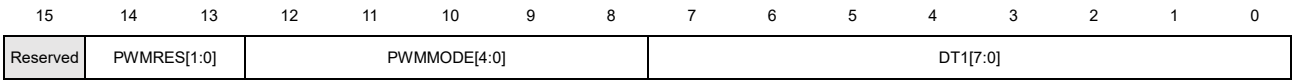
6.2.2 Register Map

Address : 0Bh



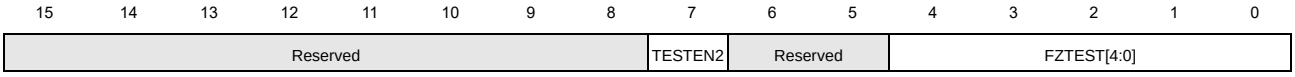
Bits	Fields	Descriptions
9	MODESEL_FZ	VD_FZ polarity selection
8	MODESEL _IRIS	VD_IS polarity selection
7	TESTEN 1	Test mode enable 1
4:3	ASWMODE[1:0]	ADTESTIN pin connection selection

Address : 20h



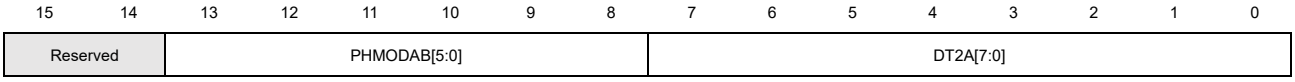
Bits	Fields	Descriptions
14:13	PWMRES[1:0]	Micro step output PWM resolution
12:8	PWMMODE[4:0]	Micro step output PWM frequency
7:0	DT1[7:0]	Start point wait time

Address : 21h



Bits	Fields	Descriptions
7	TESTEN2	Test mode enable 2
4:0	FZTEST[4:0]	PLS1/2 pin output signal selection

Address : 22h



Bits	Fields	Descriptions
13:8	PHMODAB[5:0]	α motor phase correction
7:0	DT2A[7:0]	α motor start point excitation wait time

Address : 23h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPWB[7:0]								PPWA[7:0]							

Bits	Fields	Descriptions
15:8	PPWB[7:0]	Driver B peak pulse width
7:0	PPWA[7:0]	Driver A peak pulse width

Address : 24h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		MICROAB[1:0]		LEDB	ENDISAB	BRAKEAB	CCWCWAB	PSUMAB[7:0]							

Bits	Fields	Descriptions
13:12	MICROAB[1:0]	α motor sine wave division number
11	LEDB	LED B output control
10	ENDISAB	α motor enable/disable control
9	BRAKEAB	α motor brake
8	CCWCWAB	α motor rotation direction
7:0	PSUMAB[7:0]	α motor step count number

Address : 25h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTCTAB[15:0]															

Bits	Fields	Descriptions
15:0	INTCTAB[15:0]	α motor step cycle

Address : 27h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		PHMODCD[5:0]						DT2B[7:0]							

Bits	Fields	Descriptions
13:8	PHMODCD[5:0]	β motor phase correction
7:0	DT2B[7:0]	β motor start point excitation wait time

Address : 28h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPWD[7:0]								PPWC[7:0]							

Bits	Fields	Descriptions
15:8	PPWD[7:0]	Driver D peak pulse width
7:0	PPWC[7:0]	Driver C peak pulse width

Address : 29h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved		MICROCD[1:0]		LEDA	ENDISCD	BRAKECD	CCWCW CD	PSUMCD[7:0]							

Bits	Fields	Descriptions
13:12	MICROCD[1:0]	β motor sine wave division number
11	LEDA	LED A output control
10	ENDISCD	β motor enable/disable control
9	BRAKECD	β motor brake
8	CCWCWCD	β motor rotation direction
7:0	PSUMCD[7:0]	β motor step count number

Address : 2Ah

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INTCTCD[15:0]															

Bits	Fields	Descriptions
15:0	INTCTCD[15:0]	β motor step cycle

Address : 2Ch

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved													INSWICH	IN1	IN2

Bits	Fields	Descriptions
2	INSWICH	DC Motor input mode select
1	IN1	DC Motor input 1
0	IN2	DC Motor input 2

6.2.3 Serial Interface Specifications

- Data transfer starts at the rising edge of CS, and stops at the falling edge of CS.
- One unit of data is 24 bits. (24 bits of the following format are called a data set in this book.)
- Address and data are serially input from SIN pin in synchronization with the data clock SCK at CS = 1.
- Data is retrieved at the rising edge of SCK.
- Moreover, data is output from SOUT pin at data readout. (Data is output at the rising edge of SCK.)
- SOUT outputs Hi-Z at CS = 0, and outputs "0" except data readout at CS = 1.
- The control circuit of serial interface is reset at CS = 0.

6.2.4 Data Format

0	1	2	3	4	5	6	7
A0	A1	A2	A3	A4	A5	C0	C1

8	9	10	11	12	13	14	15
D0	D1	D2	D3	D4	D5	D6	D7

16	17	18	19	20	21	22	23
D8	D9	D10	D11	D12	D13	D14	D15

- C0 : Register write / read selection 0 : write mode, 1 : read mode
- C1 : Unused
- A5 to A0 : Address of register
- D15 to D0 : Data written in register

When C0 bit is "0", the write mode is selected. The address and data are retrieved from SIN in synchronization with the rising edge of data clock SCLK, and the data is stored in internal register in synchronization with the rising edge of CS.

SOUT outputs "0" in the write mode.

When the data which is 23 or less bits per 1 processing is received in the write mode, the received data becomes invalid. The data of 25 or more bits is regarded as the continuous write mode, and the write operation is performed whenever the data of 24 bits is received. When the last data set is less than 24 bits in the continuous write mode, it becomes invalid. (The previous data set is valid.)

Even if noise occurs on SCK signal in the continuous write mode and the shifted data is received, pay attention to continue receiving or updating the shifted data.

When C0 bit is "1", the read mode is selected. The address is retrieved from SIN in synchronization with the rising edge of SCK, and then the register value of the address specified is output as LSB first from SOUT, in synchronization with the rising edge of SCK.

When C0 bit is "1", the values of D15 to D0 of SIN do not be cared.

6.2.5 Formatting

All the SIF functions containing a data register are formatted at RSTB = 0. Characteristic of supply voltage monitor.

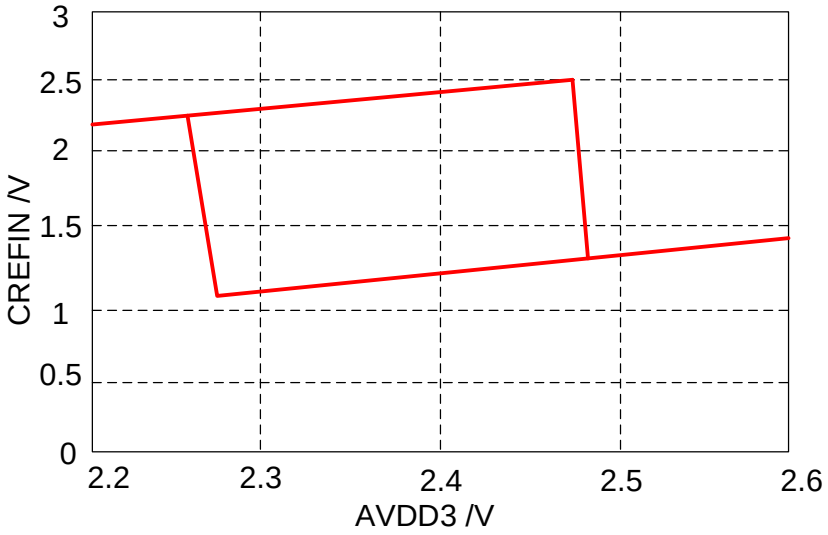


Figure 4 AVDD3 (Operation voltage:2.28V Return voltage: 2.48V)

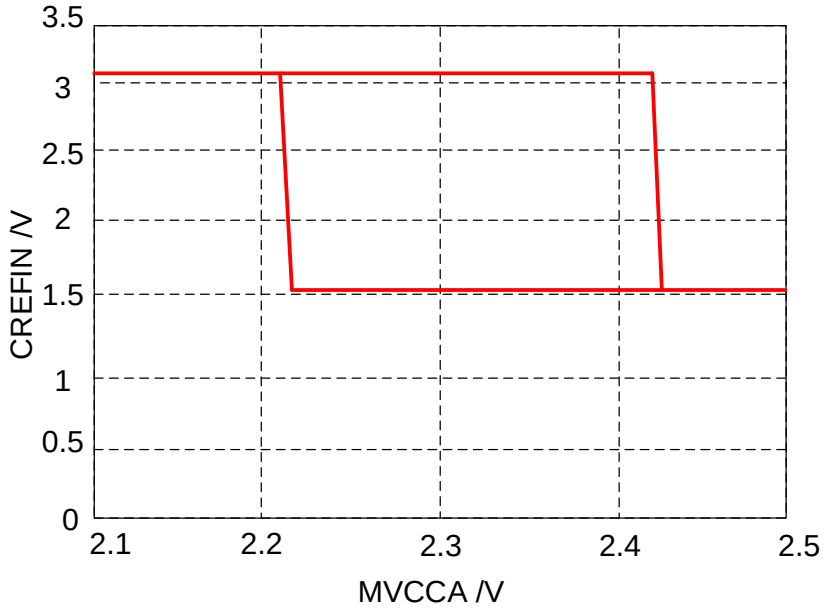


Figure 5 MVCC (Operation voltage:2.22V Return voltage: 2.42V)

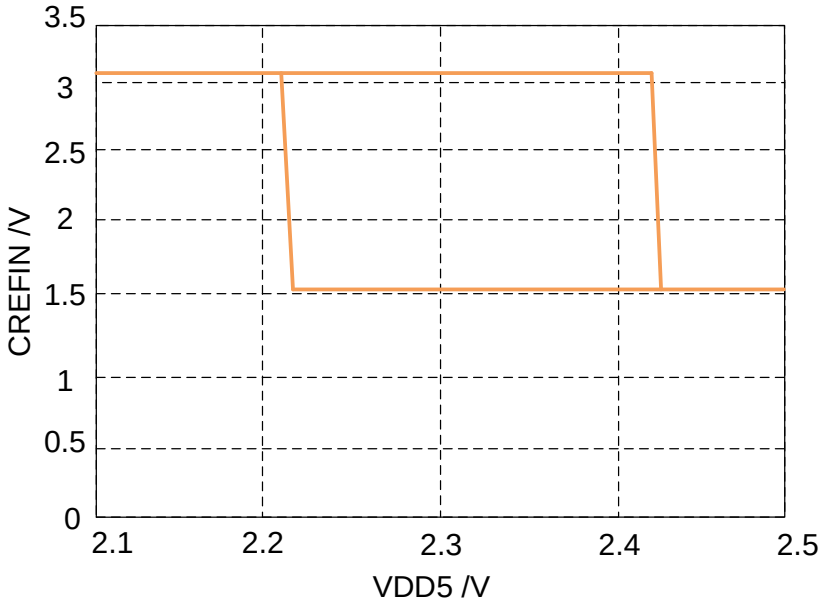
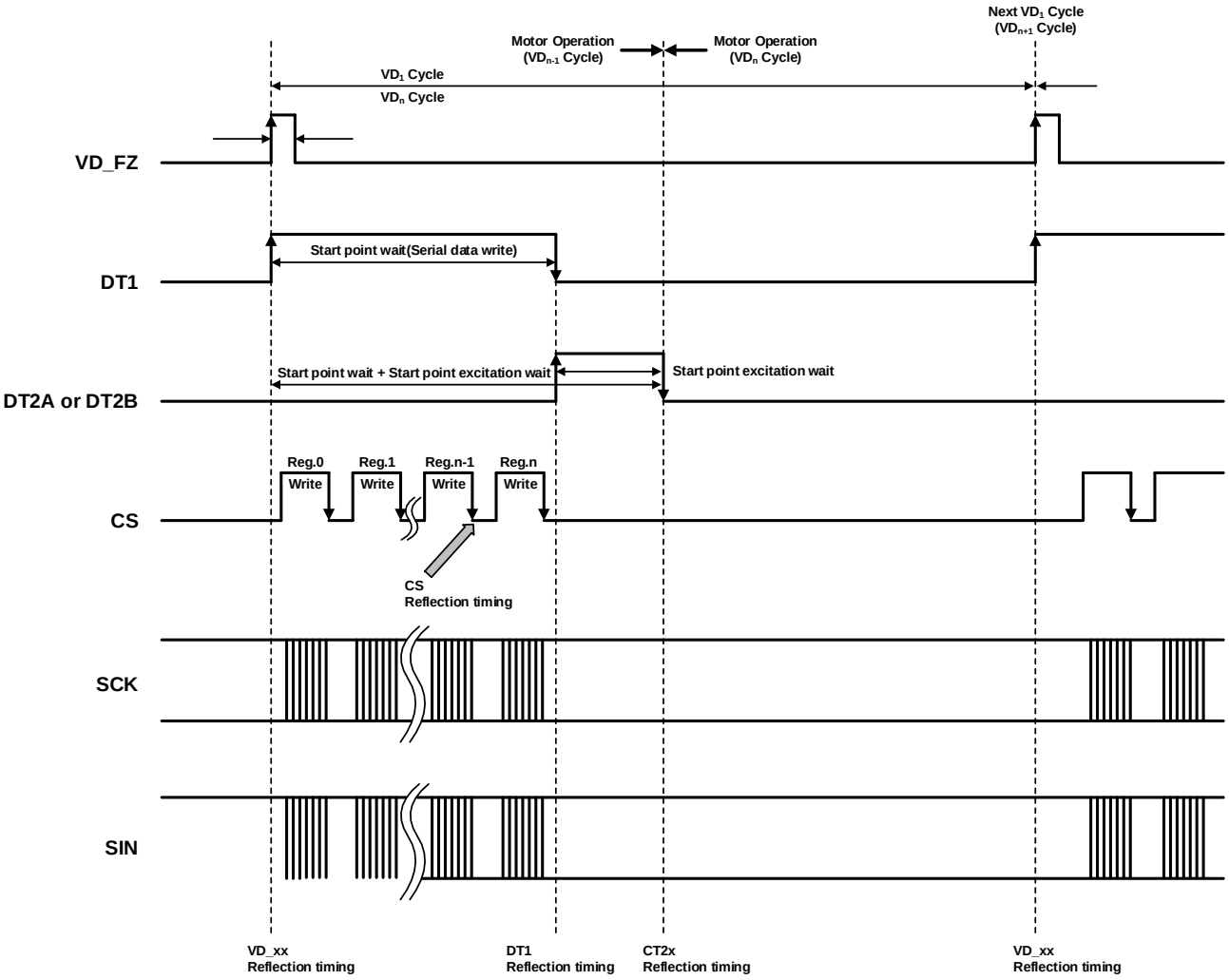


Figure 6 VDD5 (Operation voltage:2.22V Return voltage: 2.42V)

6.2.6 Register Setup Timing



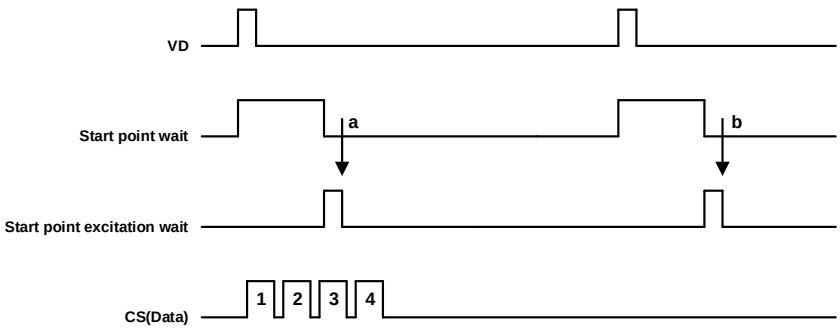
Address	Register Name	Setup Timing
0Bh	TESTEN1	CS
	MODESEL_FZ	CS
20h	DT1[7:0]	VD_FZ
	PWMMODE[4:0]	DT1
	PWMRES[1:0]	DT1
21h	FZTEST[4:0]	CS
	TESTEN2	CS
22h	DT2A[7:0]	DT1
	PHMODAB[5:0]	DT2A
23h	PPWA[7:0]	DT1
	PPWB[7:0]	DT1
24h	PSUMAB[7:0]	DT2A

Address	Register Name	Setup Timing
	CCWCWAB	DT2A
	BRAKEAB	DT2A
	ENDISAB	DT1 or DT2A*
	LEDB	CS
	MICROAB[1:0]	DT2A
25h	INTCTAB[15:0]	DT2A
27h	DT2B[7:0]	DT1
	PHMODCD[5:0]	DT2B
28h	PPWC[7:0]	DT1
	PPWD[7:0]	DT1
29h	PSUMCD[7:0]	DT2B
	CCWWCD	DT2B
	BRAKECD	DT2B
	ENDISCD	DT1 or DT2B[1]
	LEDA	CS
	MICROCD[1:0]	DT2B
2Ah	INTCTCD[15:0]	DT2B
2Ch	INSWICH	CS
	IN1	CS
	IN2	CS

1. 0 → 1: reflected at DT1 1 → 0: reflected at DT2x

In principle, the setup of registers for micro step should be performed during the interval of start point wait (Refer to the figure in page 18). The data which is written at timing except the interval of start point wait can be also received. However, if the write operation continues after the reflecting timing such as the end of start point excitation wait, the setup reflection timing may not be performed at the intended timing (Refer to the following figure).

For example, if the data 1 to 4 which is updated at the end of start point excitation wait are written as the following figure, data 1 and 2 is updated at the timing a, and data 3 and 4 is updated at the timing b. Even if the data is written continuously like this, the update timing may be shifted to 1 VD. Due to the above reason, the setup of registers should be performed during the interval of start point wait in order to reflect the updated content certainly.



6.3 VD Signal Internal Processing

6.3.1 Specifications

In this LSI, reflection timing and rotation timing of a stepping motor are based on the rising edge of VD_FZ respectively. The polarities of VD_FZ which are used for the internal processing can be set by the following setup.

6.3.2 Register detail description

- **MODESEL_FZ (VD_FZ polarity selection)**

Adress			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							MODESEL_FZ								

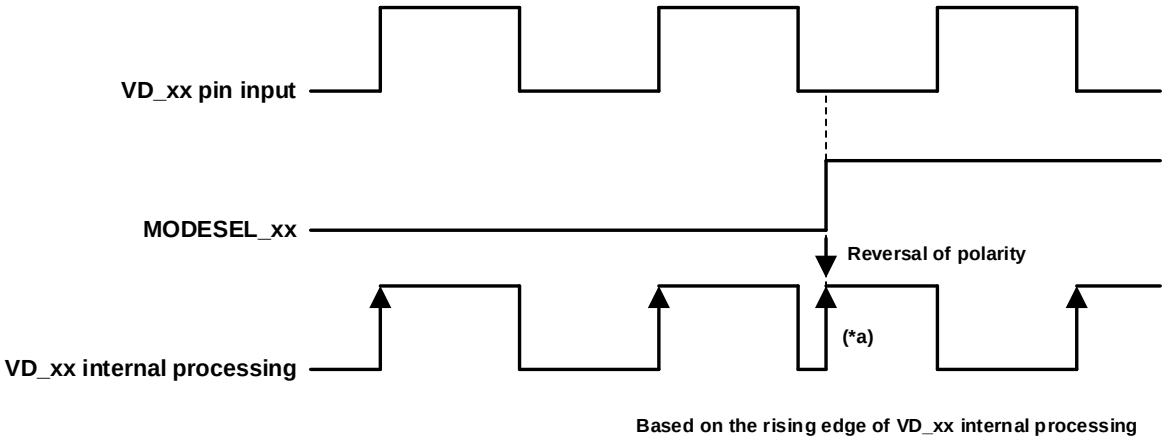
MODESEL_FZ respectively set the polarities of VD_FZ signals which is input to this IC.

When setting to "0", the polarity is based on the rising edge of VD_FZ inputted.

When setting to "1", the polarity is based on the falling edge of VD_FZ inputted.

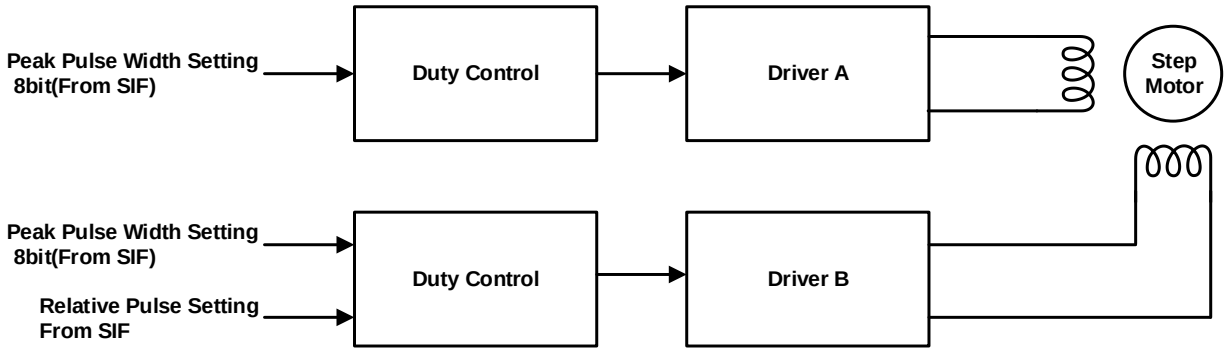
MODESEL_xx selects the polarity of VD_xx inputted. Therefore, depending on the selection timing of MODESEL_xx, the timing which is not related to the edge (*a) of VD_xx which is input as the following figure may be regarded as an edge.

Setup value	VD polarity
0	Non-inverting
1	Inverting



6.4 Micro Stepping Motor Driver

This block is a stepping motor driver for focus and zoom, and the following setup can be performed by serial control. (The following description is for α motor: driver A/B. β motor: driver C/D is the same function as α motor).



Main setup parameters

1) Phase correction : The phase difference between a driver A and a driver B is on the basis of 90 degree, and can be adjusted from –22.5 degree to +21.8 degree.(PHMODAB[5:0])
2) Amplitude correction : It is possible to set the load current of driver A/B independently. (PPWA[7:0], PPWB[7:0])
3) PWM frequency : PWM driver chopping frequency is set.(PWMMODE[4:0], PWMRES[1:0])
4) Quasi-sine wave : Number of divisions can be set to 64, 128 and 256. (MICROAB[1:0])
5) Stepping cycle : Motor rotation speed is set. The rotation speed is constant regardless of number of divisions of quasi-sine wave.(INTCTAB[15:0])

6.4.1 Electrical Characteristics at AVDD5, MVCCx = 4.8V, DVDD, AVDD3 = 3.1V

T_A = 25°C ± 2°C(unless otherwise specified).

SYMBOL	PARAMETER	CONDITIONs	MIN	TYP	MAX	UNIT
MOTOR DRIVER 1 (FOCUS, ZOOM)						
R_{onFZ}	H bridge ON resistance	IM=100mA	0.6	0.8	1.4	Ω
I_{leakFZ}	H bridge leak current				0.8	uA

6.4.2 Setup Timing for Each Setup

Setup timing and number of times are shown as follows. Since the setups for address 27h to 2Ah are the same as those of 22h to 25h, the descriptions for address 27h to 2Ah are omitted. If each setup is set once, the setup is reflected at every VD pulses. Therefore, when the same setup is performed at two or more VD pulses, it is unnecessary to write at every VD pulse.

DT1[7:0] (Start point wait, Address 20h)

Update timing is set. After hard reset release (RSTB : Low → High), this setup should be performed before starting to excite and drive a motor. Since this setup is updated by the start of VD, it is unnecessary to write during the start point wait.

PWMMODE[4:0]，PWMRES[1:0] (Micro step output PWM frequency setup，Address 20h)

Micro step output PWM frequency is set. After hard reset release (RSTB : Low to High), this setup should be performed before starting to excite and drive a motor (DT1 ends).

DT2A[7:0] (Start point excitation wait, Address 22h)

Updated timing is set. After hard reset release (RSTB : Low → High), this setup should be performed before

starting to excite and drive a motor (DT1 ends).

PHMODAB[5:0] (Phase correction, Address 22h)

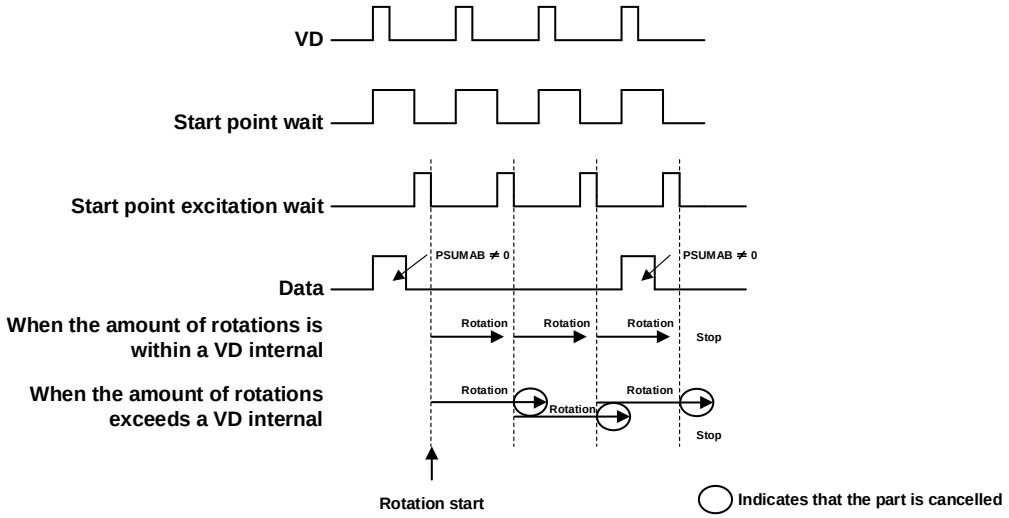
The correlation phase difference between coil A and B is corrected, and the driving noise is reduced. Since the amount of suitable phase correction depends on the rotation direction or rotation speed, the change of this setup should be performed simultaneously with the changes of the rotations direction (CCWCWAB) or rotation speed (INTCTAB), or it should be performed when a motor does not rotate.

PPWA[7:0]，PPWB[7:0] (Peak pulse width, Address 23h)

PWM maximum duty is set. This setup should be performed before starting to excite and drive a motor (DT1 ends).

PSUMAB[7:0] (Step count number, Address 24h)

The amount of motor rotations in 1 VD interval is set. Every time VD pulse is input, the motor keeps rotating depending on the amount of rotations. Therefore, set to "0" in order to stop rotation of the motor. When the amount of rotations which exceeds 1 VD interval is set, the amount of rotations of a part which exceeds 1 VD interval is cancelled.



CCWCWAB (Rotation direction, Address 24h)

Rotation direction is set. This setup should be performed just before switching the rotation direction.

BRAKEAB (Brake setup, Address 24h)

A current is set to 0 by braking. Since it becomes impossible to get the excitation position of a motor by braking, this setup should not be preformed except for the case of stopping immediately.

ENDISAB (Motor enable/disable setup, Address 24h)

Enable of a motor is set. Since a motor pin is Hi-Z when it is set to "Disable", do not set to "Disable" while a motor keeps rotating.

LEDA (LED setup, Address 24h)

LED ON/OFF is set. The setup is performed at the falling edge of CS.

(It is understood that it is not related to driving a motor. It is possible to turn ON/OFF independently.)

MICROAB[1:0] (Number of sine wave divisions, Address 24h)

Number of sine wave divisions is set. Even if this setup is changed, the amount of rotations and rotation speed do not vary.

If only the control which the number of divisions varies depending on the rotation speed is not performed, the problem dose not occur if it is set once after hard reset release (RSTB : Low → High).

INTCTAB[15:0] (Pulse cycle, Address 25h)
Pulse cycle is set. Rotation speed is determined by this setup.

6.4.3 How to adjust register setting for micro stepping motor driver

In order to control lens, it is required to set motor rotation speed and amount of rotation per VD. Register settings relating to speed and amount of rotation are:

1. INTCTxx[15:0]: set time of each step (that is, the rotation speed)
2. PSUMxx[7:0]: amount of rotation per VD period

When driving the motor continuously for several VD period, it is best to match rotation time (per VD) to VD period. Below is a method to calculate INTCTxx[15:0] and PSUMxx[7:0] for smooth motor rotation.

1) Calculate INTCTxx[15:0] from desired rotation speed.

$$\text{INTCTxx[15:0]} \times 768 = \frac{\text{OSCIN frequency}}{\text{rotation frequency}}$$

2) Calculate PSUMxx[7:0] from INTCTxx[15:0]. Round off if the result of PSUMxx[7:0] is not integer.

When the below equation is satisfied, the rotation time is equal to VD period, and smooth rotation is realized.

$$\text{INTCTxx[15:0]} \times \text{PSUMxx[7:0]} \times 24 = \frac{\text{OSCIN frequency}}{\text{VD frequency}}$$

3) If PSUMxx[7:0] is rounded off, recalculate INTCTxx[15:0] from the equation in 2).

Example: OSCIN frequency = 27 MHz, VD frequency = 60 Hz

Calculate PSUMxx[7:0] and INTCTxx[15:0] to rotate motor at 800 pps (1-2 phase). 800 pps = 100 Hz, so from equation in 1),

$$\text{INTCTxx[15:0]} = \frac{27\text{MHz}}{(100\ \text{Hz} \times 768)} = 352$$

Next, calculate PSUMxx[7:0] from equation in 2):

$$\text{PSUMxx[7:0]} = \frac{1}{60\ \text{Hz}} \times \frac{27\ \text{MHz}}{352 \times 24} = 53$$

Since PSUMxx[7:0] is rounded off, recalculate INTCTxx[15:0] from equation in 2):

$$\text{INTCTxx[15:0]} = \frac{1}{60\ \text{Hz}} \times \frac{27\ \text{MHz}}{53 \times 24} = 354$$

Refer to pages 23 and 28 for detail of PSUMxx[7:0] and INTCTxx[15:0].

If the value of left-hand side in 2) is smaller than right-hand side, the rotation time will be shorter than VD period and will cause discontinuous rotation. If left-hand side is smaller, the rotation time that exceeds 1 VD will be cancelled.

6.4.4 Detail descriptions of register

- DT1[7:0] (Start point wait time)

Address			20h			Initial Value			0Ah						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT1[7:0]							

DT1[7:0] sets the delay time (start point wait time) until the data written in the serial data communication sends to the output.

It becomes possible to excite a motor after a start point wait switches "1" to "0". The start point wait starts to count after the rising edge of video sync signal (VD_FZ).

Since start point wait time is the trigger required for data acquisition, be sure to set to other than "0". When the value of register is "0", the data cannot be updated.

Refer to page 10 for the relationship of VD_FZ and start point wait time.

DT1	Start point wait
0	Prohibition
1	303.4us
255	77.4ms
n	n X 8192 / 27MHz

- DT2A[7:0] (Start point excitation wait α motor)

Address			22h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2A[7:0]							

- DT2B[7:0] (Start point excitation wait β motor)

Address			27h			Initial Value			03h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								DT2B[7:0]							

DT2A[7:0] and DT2B[7:0] set the delay time (start point excitation wait) until α motor and β motor start rotation. Motor rotation starts after start point excitation wait switches "1" to "0". The start point excitation wait starts to count after the falling edge of start point wait.

Since the falling edge is the trigger pulse which is required for data acquisition, be sure to input the data of other than "0". When the value of register is "0", the data cannot be updated.

Refer to page 17 for the relationship of VD_FZ and start point excitation wait time.

Setup value	Start point excitation wait
0	Prohibition
1	303.4us
255	77.4ms
n	n X 8192 / 27MHz

- PWMMODE[4:0] (Micro step output PWM frequency)

Address			20h			Initial Value			1Ch						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			PWMMODE[4:0]												

- PWMMODE[4:0] (Micro step output PWM frequency)

Address			20h			Initial Value			1h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
	PWMRES														

PWMMODE[4:0] sets the frequency division value of system clock, OSCIN, which is used as the standard of PWM signal for micro step output. PWMMODE[4:0] can set in the range from 1 to 31. PWM frequency at PWMMODE = 0 is the same as that at PWMMODE = 1.

PWMRES[1:0] sets the resolution of frequency division value set by PWMMODE[4:0]. PWM frequency is calculated by the following formula.

$$\text{PWM frequency} = \frac{OSCIN\ \ frequency}{((PWMMODE\ \times\ 2\ ))}$$

Refer to next part for the specific PWM frequency set by PWMMODE[4:0] and PWMRES[1:0] at OSCIN = 27MHz. PWM frequency setup. PWM frequency for OSCIN = 27 MHz is shown in below table.

PWMMODE	PWMRES			PWMMODE	PWMRES		
	0	1	2		0	1	2
1	3375.0	1687.5	843.8	17	198.5	99.3	49.6
2	1687.5	843.8	421.9	18	187.5	93.8	46.9
3	1125.0	526.5	281.3	19	177.6	88.8	44.4
4	843.8	421.9	210.9	20	168.8	84.4	42.2
5	675.0	337.5	168.8	21	160.7	80.4	40.2
6	526.5	281.3	140.6	22	153.4	76.7	38.4
7	482.1	241.1	120.5	23	146.7	73.4	36.7
8	421.9	210.9	105.5	24	140.6	70.3	35.2
9	375.0	187.5	93.8	25	135.0	67.5	33.8
10	337.5	168.8	84.4	26	129.8	64.9	32.5
11	306.8	153.4	76.7	27	125.0	62.5	31.3
12	281.3	140.6	70.3	28	120.5	60.3	30.1
13	259.6	129.8	64.9	29	116.4	58.2	29.1
14	241.1	120.5	60.3	30	112.5	56.3	28.1
15	225.0	112.5	56.3	31	108.9	54.4	27.2
16	210.9	105.5	52.7				

- PHMODAB[5:0] (Phase correction α motor)

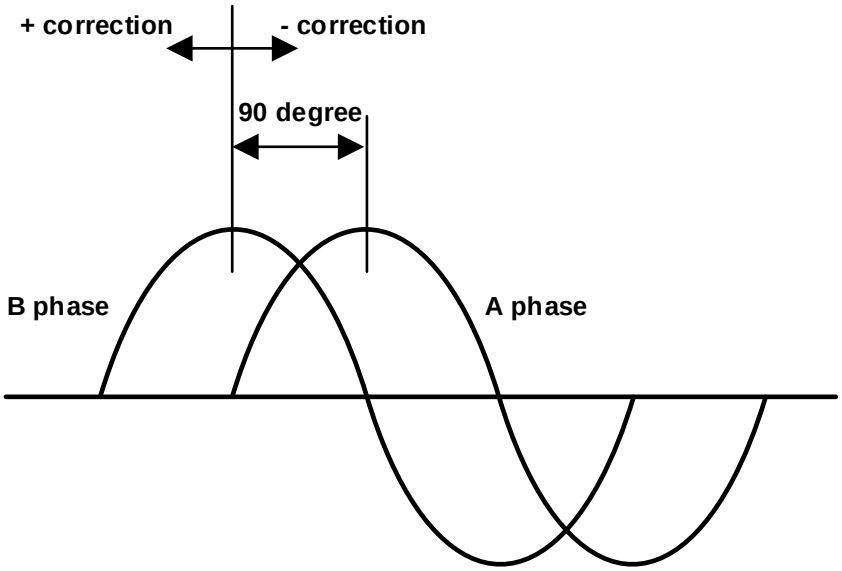
Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODAB[5:0]													

- PHMODCD[5:0] (Phase correction β motor)

Address			22h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		PHMODCD[5:0]													

Current phase differences of α motor and β motor shifts from 90 degree by PHMODAB[5:0] and PHMODCD[5:0] respectively. Setup resolution is 0.7 degree, and data is set in two's complement.

PHMODCD	Amount of phase correction
000000	±0°
000001	+0.7°
011111	+21.80°
100000	-22.50°
111111	-0.7°
Resolution	360°/512 = 0.7°



Stepping motor is configured so that phase difference between coils becomes 90 degree. However, the phase difference may shift from 90 degree due to the variation of a motor.

Therefore, even if phase difference in current waveform is exactly 90 degree, driving noise may occur due to the occurrence of rotation torque ripple.

This setup is for reducing the torque ripple which is occurred by the variation of a motor.

- PPWA[7:0]（Driver A peak pulse width）
- PPWB[7:0]（Driver B peak pulse width）

Address			23h			Initial Value			0, 0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWA[7:0]								PPWB[7:0]							

- PPWC[7:0] (Driver B peak pulse width)
- PPWD[7:0] (Driver D peak pulse width)

Address			28h			Initial Value			0, 0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PPWC[7:0]									PPWD[7:0]						

PPWA[7:0] to PPWD[7:0] set the maximum duty of PWM at the position which the currents in driver A to D are peak value respectively. The maximum duty is calculated by the following formula.

$$\text{Driver X Maximum duty} = \frac{\text{PPWx}}{(\text{PWMMODE} \times 8)}$$

When PPWx = 0 is set, coil current becomes 0.

Example: When PPWA[7:0] = 200, PWMMODE[4:0] = 28 is set, maximum duty of driver A will be

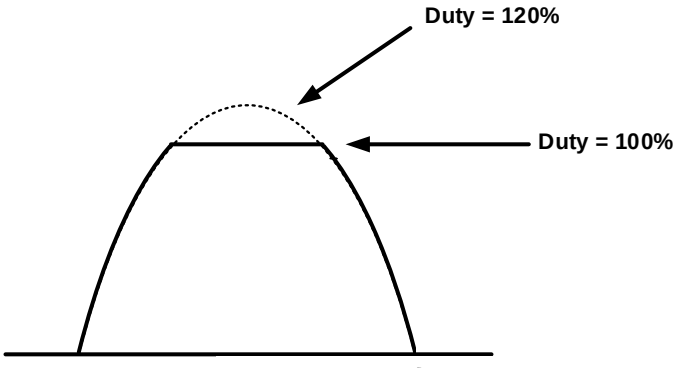
$$\frac{200}{(28 \times 8)} = 0.89$$

Maximum duty may exceed 100% depending on the setup values of PWMMODE and PPWx.

Since the duty does not certainly exceed 100% at PWM operation in this case, the peak point of sine wave (current waveform) becomes flat as follows.

Example 1 : When PWMMODE = 10, PPWx = 96, Maximum duty = 96 / (10 × 8) = 120%

The target current waveform is indicated as the following full line.



- PSUMAB[7:0]（α motor step count number）

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMAB[7:0]							

- PSUMCD[7:0]（β motor step count number）

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								PSUMCD[7:0]							

PSUMAB[7:0] and PSUMCD[7:0] set the number of step counts of α motor and β motor respectively.

Since the number of setup step counts is converted to 256-step inside, the amount of rotation becomes the same regardless of the number of divisions.

To stop the rotation of a motor, set PSUMxx[7:0] = 0.

Setting value	Number of steps		
	64-step conversion	128-step conversion	256-step conversion
0	0	0	0
1	2	4	8
255	510	1020	2040
n	2n	4n	8n

If maximum duty is set to other than "0" at PSUMxx[7:0] = 0, the position is held in the state of excitation.

If a motor can hold the position by cogging torque without motor current, the position is held even if the maximum duty is set to 0.

Example: When PSUMAB[7:0] = 8 is set, the amount of rotation is 16 steps (64-step conversion).

This is 16/64 =1/4 of a sine wave. The amount of rotation becomes 1/4 of a sine wave also in 128 and 256-step conversion.

- CCWCWAB（α motor rotation direction）

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWAB								

- CCWCWCD（β motor rotation direction）

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
							CCWCWCD								

CCWCWAB and CCWCWCD set the rotation direction of α motor and β motor respectively.

Setup value	Motor rotation direction
0	Forward
1	Reverse

- BRAKEAB（α motor brake）

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						ERAKEAB									

- BRAKECD（β motor brake）

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
						ERAKECD									

BRAKEAB and BRAKECD set the brake mode of α motor and β motor respectively.

Setup value	Motor brake
0	Normal operation
1	Brake mode

Both of upper-side P-ch MOSs of output H bridge turn on in brake mode. The brake mode is not used in normal

operation, and is used for emergency shutdown. It is recommended to use only in abnormal state.

- ENDISAB（α motor Enable/Disable）

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISAB										

- ENDISCD（β motor Enable/Disable）

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
					ENDISCD										

ENDISAB and ENDISCD configure the setting for output stage control of α motor and β motor respectively.

The output becomes the state of OFF (Hi-Z) at ENDISxx = 0. However, internal excitation position counter keeps counting even ENDISxx = 0. Therefore, when stopping the motor during normal operation, set PSUMxx[7:0] = 0 (not ENDISxx = 0).

Setup value	Motor output condition
0	Output OFF (Hi-Z)
1	Output ON

- MICROAB[1:0] (α motor quasi-sin wave division number)

Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROAB													

- MICROCD[1:0]（β motor quasi-sine wave division number）

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
		MICROCD													

MICROAB[1:0] and MICROCD[1:0] set the number of quasi-sine wave divisions for α motor and β motor respectively.

Setup value	Number of divisions
00	256
01	256
10	128
11	64

- INTCTAB[15:0]（α motor step cycle setup）

Address			25h			Initial Value			0080h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTAB[15:0]															

- INTCTCD[15:0]（β motor step cycle setup）

Address			2Ah			Initial Value			0080h						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
INTCTCD[15:0]															

INTCTAB[15:0] and INTCDCD[15:0] set the step cycle of α motor and β motor respectively. Since the step cycle is converted to 64-step inside, motor rotation speed becomes the same regardless of the number of divisions set by MICROxx[1:0].

Setting value	step cycle		
	64-step	128-step	256-step
0	0	0	0
1	444ns	222ns	111ns
Max	29.1ms	14.6ms	7.3ms
n	12n/27MHz	6n/27MHz	3n/27MHz

If maximum duty is set to other than "0" at INTCTxx[15:0] = 0, the position is held in the state of excitation.

If a motor can hold the position by cogging torque without motor current, the position is held even if the maximum duty is set to 0.

Example: If ITCTAB[15:0] = 400 is set, time of 1 step for 64-step is

$$12\times\frac{400}{27\text{MHz}}=0.178\ \text{ms}$$

Therefore, period of one sinusoidal wave cycle is 11.4 ms (87.9 Hz).

This is the same for 128-step and 256-step.

- FZTEST[4:0] (Test signal output setup)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
											FZTEST[4:0]				

- TESTEN1(Test setting 1)

Address			0Bh			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN1							

- TESTEN2(Test setting 2)

Address			21h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
								TESTEN2							

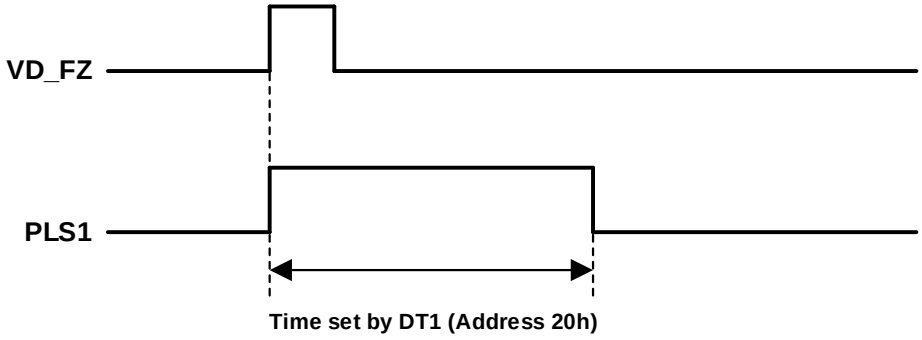
FZTEST[4:0] makes a choice of the test signal which is output to PLS1 and PLS2 pins.

TESTEN1 (0Bh) and TESTEN2 (21h) should be set to "1" in order to enable the test signal.

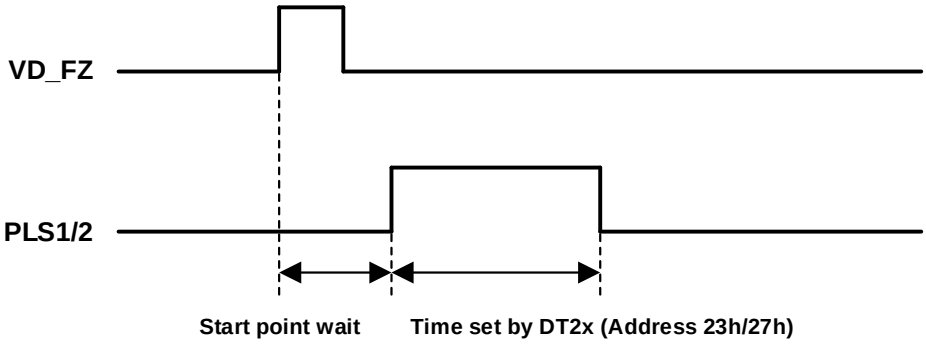
Since the test signal used in our company is output, do not set other than the setups described in the following table.

Setup value	Step cycle		Description
	PLS1	PLS2	
0	PLS1	PLS2	Pulse 1/2 normal function
1	Start point wait	0	“H” output during start point wait
2	Start point excitation wait A	Start point excitation wait B	“H” output during start point excitation wait
3	ENDISAB	ENDISCD	ENDISxx setting
4	CCWCWAB	CCWCWCD	CCWCWxx setting
5	Pulse output monitor A	Pulse output monitor B	During motor rotation, “H”/”L” changes at the speed of 64-step
6	PWM cycle monitor	0	PWM frequency signal for micro step
7	Pulse completion output A	Pulse completion output B	“H” output during motor rotation

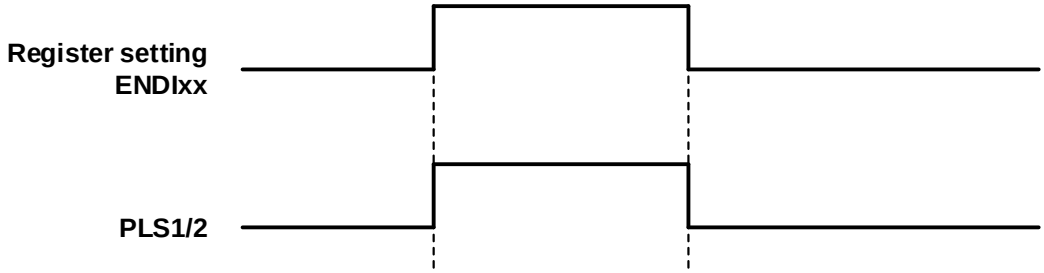
Waveform for each test signal is described below.



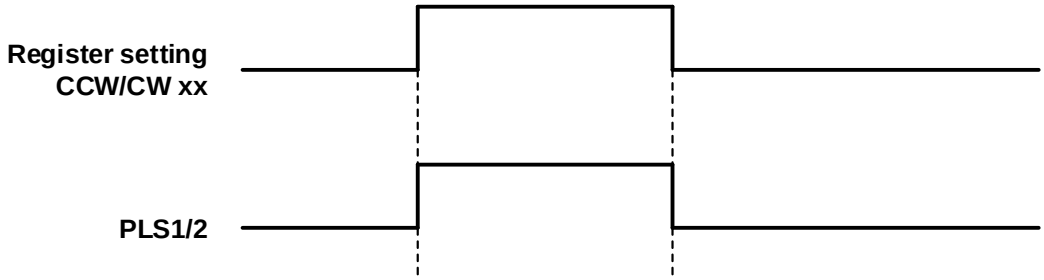
Start point excitation wait



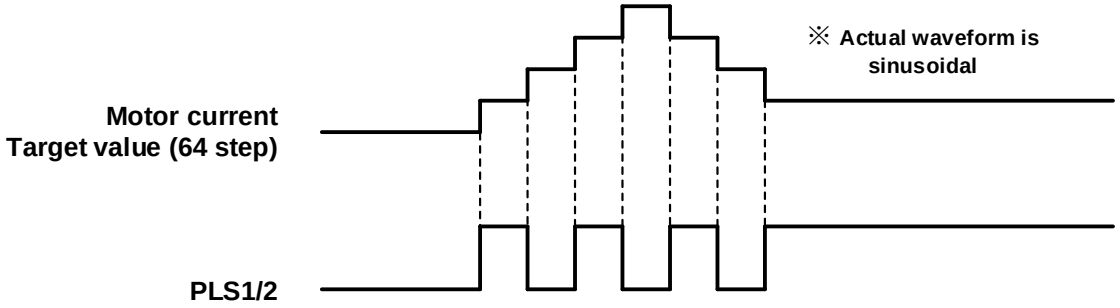
ENDISxx



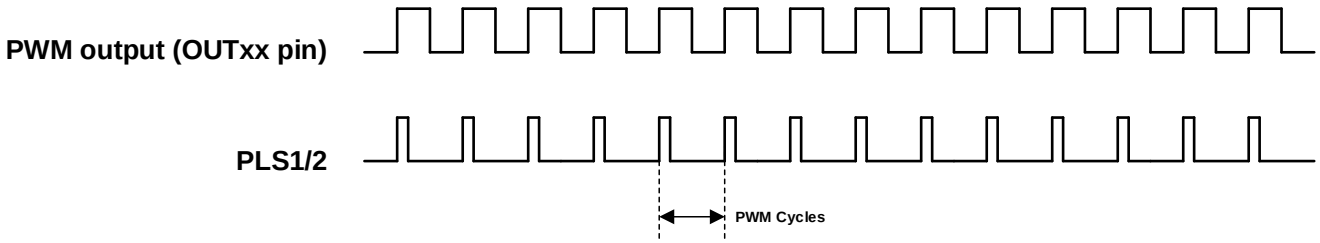
CCWCWxx



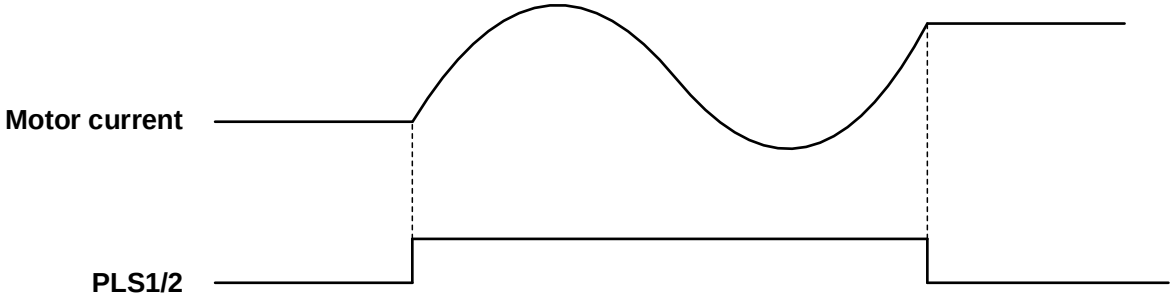
Pulse output monitor



PWM cycle monitor



Pulse completion output



6.4.5 PWM frequency setup and Maximum duty setup

The setups method example of PWM frequency and maximum duty are shown as follows.

PWM frequency setup

PWM frequency is calculated by the following formula with PWMMODE[4:0] and PWMRES[1:0] .

$$\text{PWM frequency} = \frac{\text{OSC frequency}}{((\text{PWMMODE} \times 23) \times 2\ \text{PWMRES})}$$

PWM frequency corresponding to the each setup value of PWMMODE and PWMRES.

Note that there may be two kinds of combination of the setup value corresponding to PWM frequency. For example, there are two kinds of setup to realize that PWM frequency is 56.3 kHz.

1. PWMMODE = 30，PWMRES = 1
2. PWMMODE = 15，PWMRES = 2

In such a case, PWMMODE should be set so that it is a larger value as described here in below.

Maximum duty setup

PWM output maximum duty is calculated by the following formula.

$$\text{Maximum duty} = \frac{\text{PPWx}}{(\text{PWMMODE} \times 8)}$$

For example, when PWM frequency is set as follows,

PWMMODE = 30，PWMRES = 1 → PWM frequency = 56.3 kHz

maximum duty becomes the following value by setting to PPWx = 200.

$$\frac{200}{(30 \times 8)} = 0.83$$

Since resolution of sine wave amplitude is determined by PPW setup, PWMMODE should be also set to as large a value as possible so that PPW becomes as large as possible.

6.4.6 Peak duty setup which exceeds 100%

PWM maximum duty at peak position of micro step current is determined by PWMMODE[4:0] and PPWx[7:0].

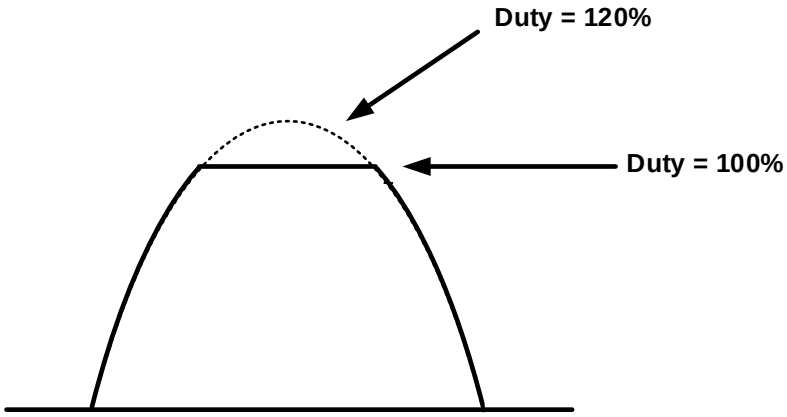
$$\text{Maximum duty} = \frac{\text{PPWx}}{(\text{PWMMODE} \times 8)}$$

Maximum duty may exceed 100% depending on the setup values of PWMMODE and PPWx.

Since the duty does not certainly exceed 100% at PWM operation in this case, the peak point of sine wave (current waveform) becomes flat as follows.

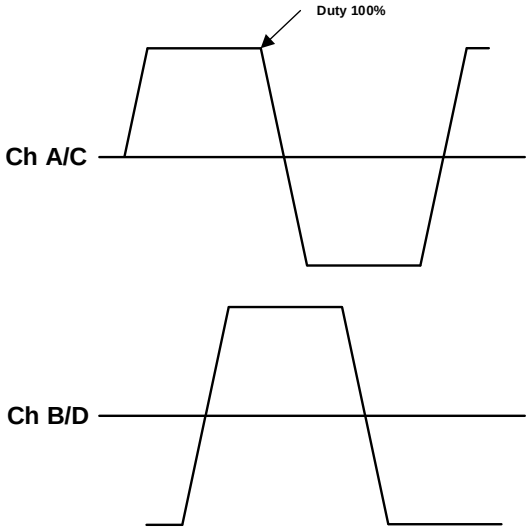
Example 1: When PWMMODE = 10, PPWx = 96, Maximum duty = 96 / (10 × 8) = 120%

The target current waveform is indicated as the following full line.

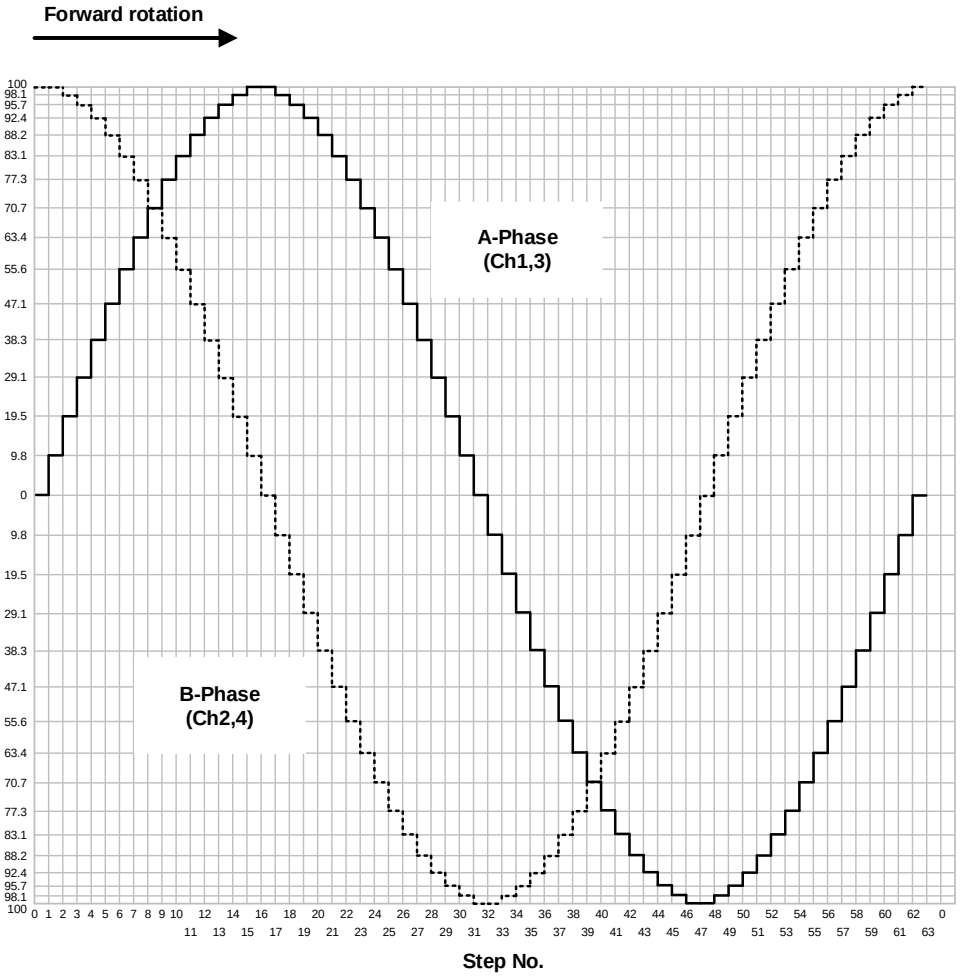


Example 2: When PWMMODE = 5, PPWx = 255, Maximum duty = 255 / (5 × 8) = 638%

The target current waveform becomes close to 2-phase drive.

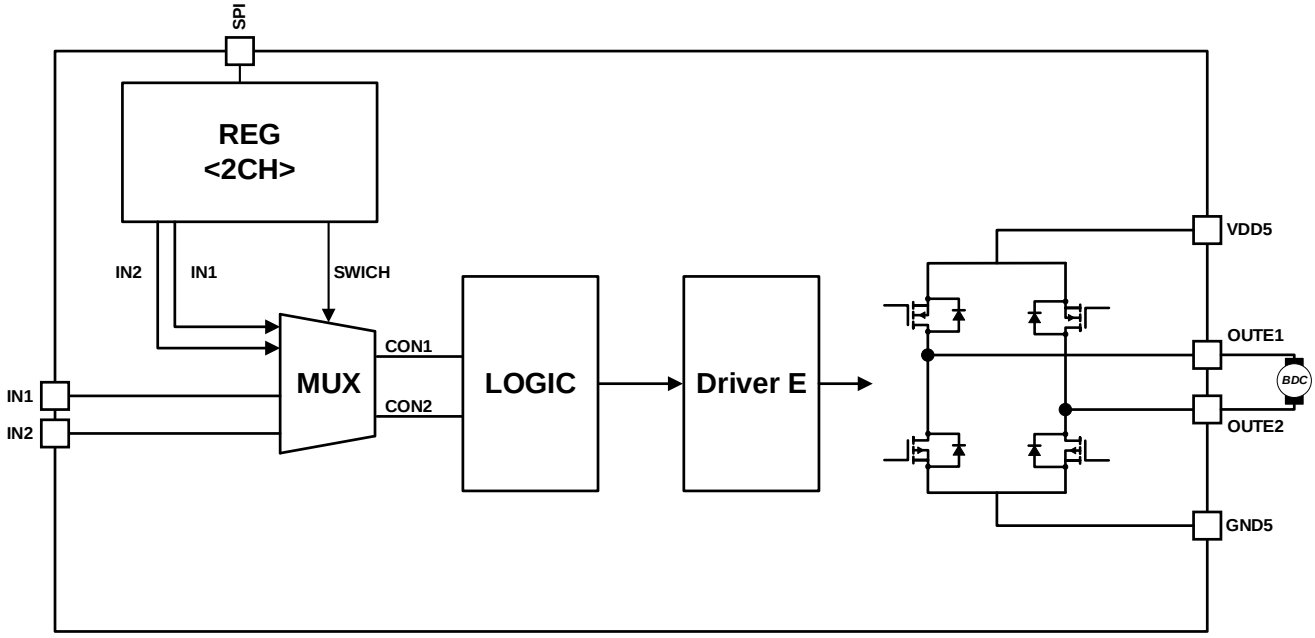


6.4.7 Micro step drive (64-step)



6.5 DC Motor Driver

This block is a DC motor driver for IR-CUT, it is driven by PWM control mode. There are two input control modes: direct external input control mode and SPI internal input control mode.



6.5.1 Electrical Characteristics

AVDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V, RL=20Ω, T_A = 25°C ± 2°C(unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
MOTOR DRIVER 2 (ir-cut) VDD5 = 5 V, RL = 20 Ω, TA = 25°C, unless otherwise noted						
R_{oncut}	R_{oncut}	R_{oncut}	R_{oncut}	R_{oncut}	R_{oncut}	Ω
$I_{leakcut}$	$I_{leakcut}$	$I_{leakcut}$	$I_{leakcut}$	$I_{leakcut}$	$I_{leakcut}$	uA
t1	Output enable time				300	ns
t2	Output disable time				300	ns
t3	Delay time, INx high to OUTx high				160	ns
t4	Delay time, INx low to OUTx low				160	ns
t5	Rise time		30		160	ns
t6	Fall time		30		188	ns
td	Delay time from SPI in to OUTE on			25*T_{SCK}	188	s

6.5.2 Detail descriptions of register

DC Motor can be controlled station by the following registers.

- INSWICH (input mode select)

Address			2Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
													INSWICH		

Setup value	state of the control	PMW	Control of the driver
0	external control (initial setting)	IN1、IN2 control	IN1、IN2 control
1	internal control	resistor control	resistor control

- IN1 (internal input control one)

Address			2Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
														IN1	

- IN2 (internal input control one)

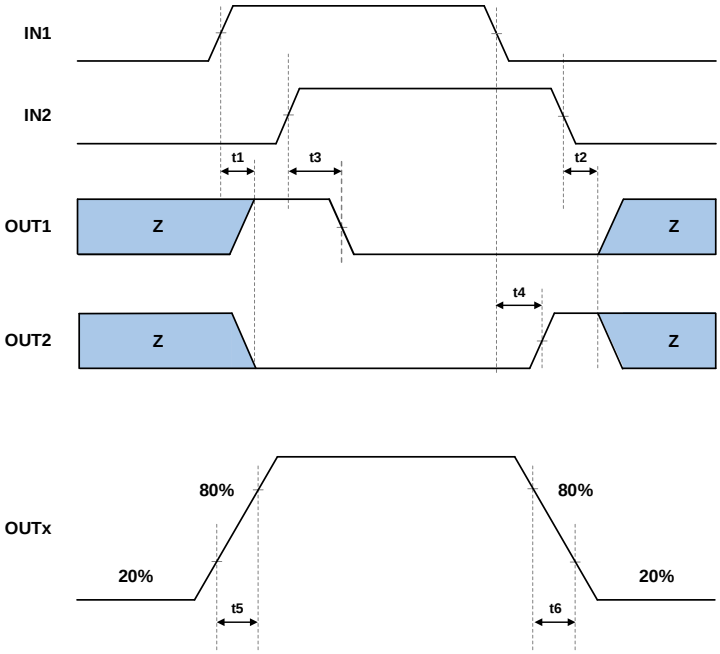
Address			2Ch			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
															IN2

IN1 and IN2 set the output station of the motor respectively.

Setup value		Output		Motor station
IN1	IN2	OUT1	OUT2	
0	0	Z	Z	Coast
0	1	L	H	Reverse
1	0	H	L	Forward
1	1	L	L	Brake

6.5.3 Detail timing requirements by the direct external input control mode

The delay time of the input to the output all less than 300ns.



6.5.4 Detail timing requirements by the SPI input control mode

Because SPI serial input writes registers (22 data and there are 3 control bits are written at a time), so the transmission delay time from writing register 2CH to the control time work is about Tsclk*25.

If the serial clock for writing data is 0.5MHz, Then the digital delay time is 25*1/0.5M=50us, at which time the maximum output frequency of H-bridge is 10KHz.

6.6 LED Driver

6.6.1 Electrical Characteristics at AVDD5, MVCCx = 4.8 V, DVDD, AVDD3 = 3.1 V

Ta = 25°C±2°C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LED DRIVER						
R_{on}LED	Output ON resistance	I=20mA, 5V cell			8.0	Ω
I_{leak}IR	Output leak current				0.8	uA

6.6.2 Detail descriptions of register

LED can be controlled ON/OFF by the following registers.

- LEDA (LED A setup)

Address			29h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDA											

- LEDB (LED B setup)

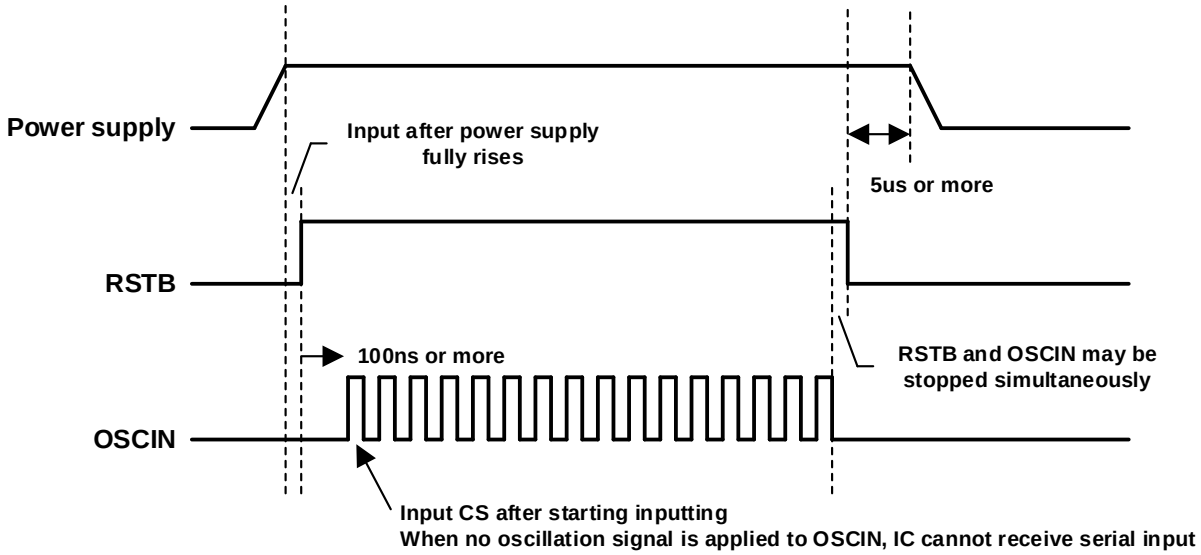
Address			24h			Initial Value			0						
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
				LEDB											

LEDA and LEDB set the output of LED A and LED B respectively.

Setup value	LED output
0	OFF
1	ON

1. Start / Stop sequence

The Start / Stop sequence of power supply, RSTB, and OSCIN is shown as follows.



2.Input capacitance of input pin

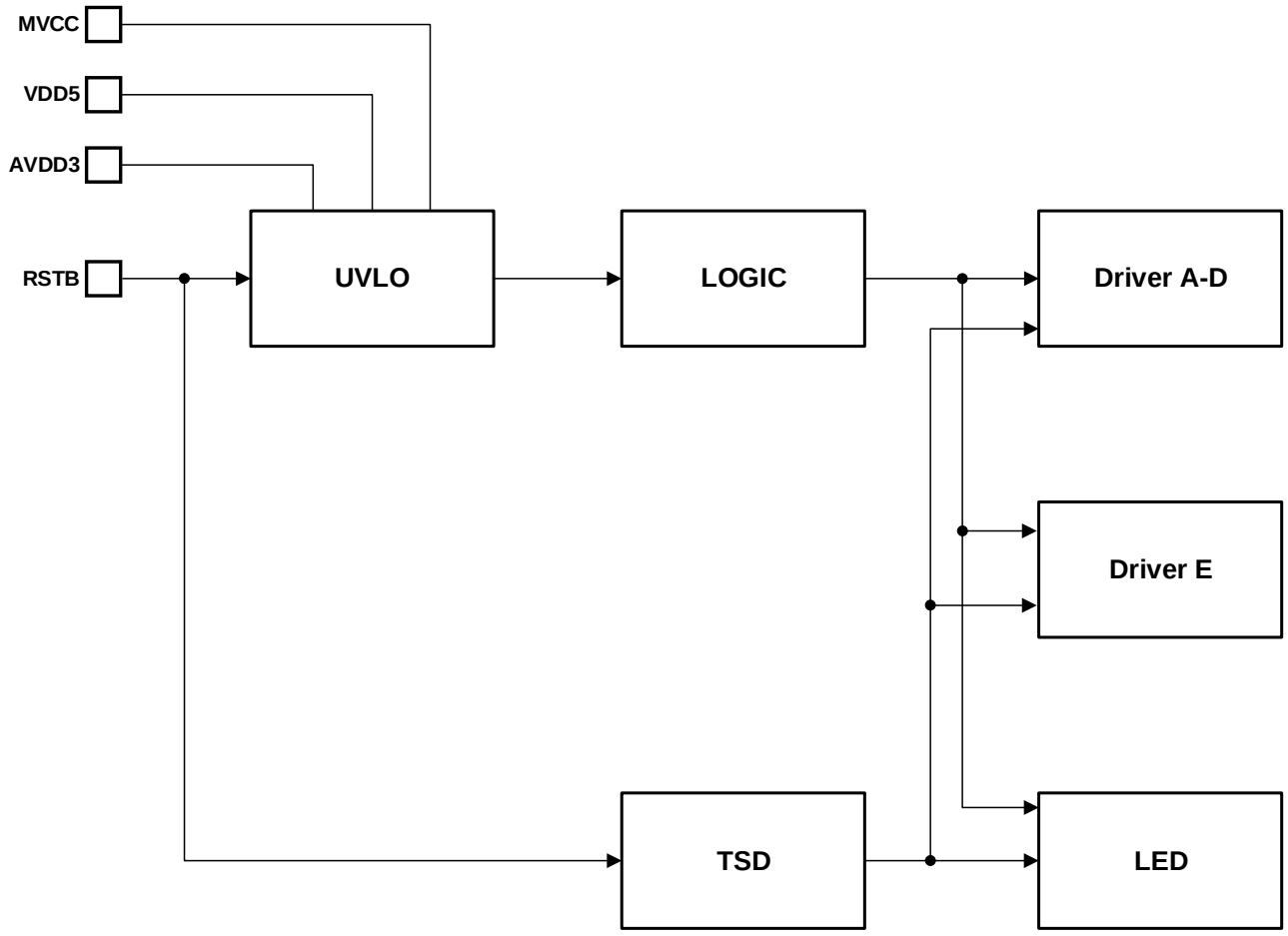
Input capacitance of input pin is 10 pF or less.

3.Timing of OSCIN and VD signal

Since the processing which VD signal (VD_FZ input) is synchronized with OSCIN is performed in this IC, OSCIN and VD signal do not have restrictions of input timing.

6.7 Reset/Protection Circuit

6.7.1 Reset/Protection Circuit Block Diagram



Stop direction (Enable → Disable) is shown as above. The specifications are shown as follows.

	COMMON	FZ output	IR-CUT output	LED
RSTB pin	Disable	Logic reset → Output OFF		
Thermal shutdown (TSD)	X	Output OFF		
Under-voltagelock-out (UVLO)	X	Logic reset → Output OFF		

1. × : Don't care
2. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault),the LSI might be damaged before the thermal protection circuit could operate.

6.7.2 Electrical Characteristics (Reference values for design)

AVDD5 = MVCCx = 4.8 V, DVDD = AVDD3 = 3.1 V, RL=20Ω, TA = 25°C ± 2°C(unless otherwise noted).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUNTDOWN						
T_{tsd}	Thermal shutdown operation temperature	Die temperature T_J		150		°C
I_{leak}IR	Thermal shutdown hysteresis width			40		°C
SUPPLY VOLTAGE MONITOR CIRCUIT						
V_{rston}	3.3 V Reset operation			2.27		V
V_{rsthys}	3.3 V Reset hysteresis			0.20		V
$V_{rstFZon}$	MVCCx Reset operation			2.20		V
$V_{rstFZhys}$	MVCCx Reset hysteresis			0.20		V
$V_{rstlSon}$	VDD5 Reset operation			2.2		V
$V_{rstlShys}$	VDD5 Reset hysteresis			0.2		V
DIGITAL INPUT						
$V_{in(H)}$	High-level input voltage			1.36		V
$V_{in(L)}$	Low-level input voltage			1.02		V
V_{hysin}	Input hysteresis width			0.34		V
$R_{pullret}$	Input pull-down resistance	RSTB		100		KΩ

1. The characteristics listed below are reference values derived from the design of the IC and are not guaranteed by inspection. If a problem does occur related to these characteristics, we will respond in good faith to user concerns.
2. Characteristic of supply voltage monitor.

7 Application Information

The GD30DR4731 is typically used to drive motors for camcoder and security cameras.

7.1 Typical Application Circuit

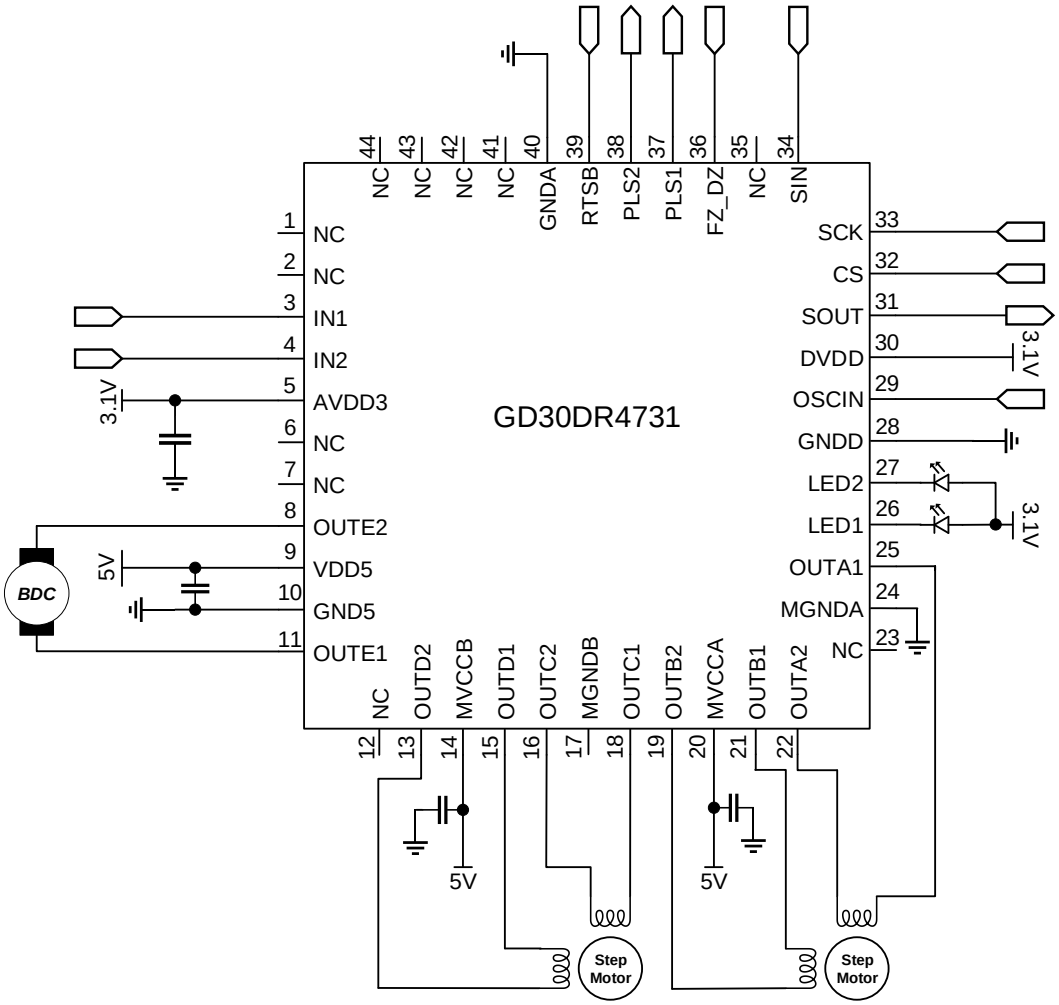
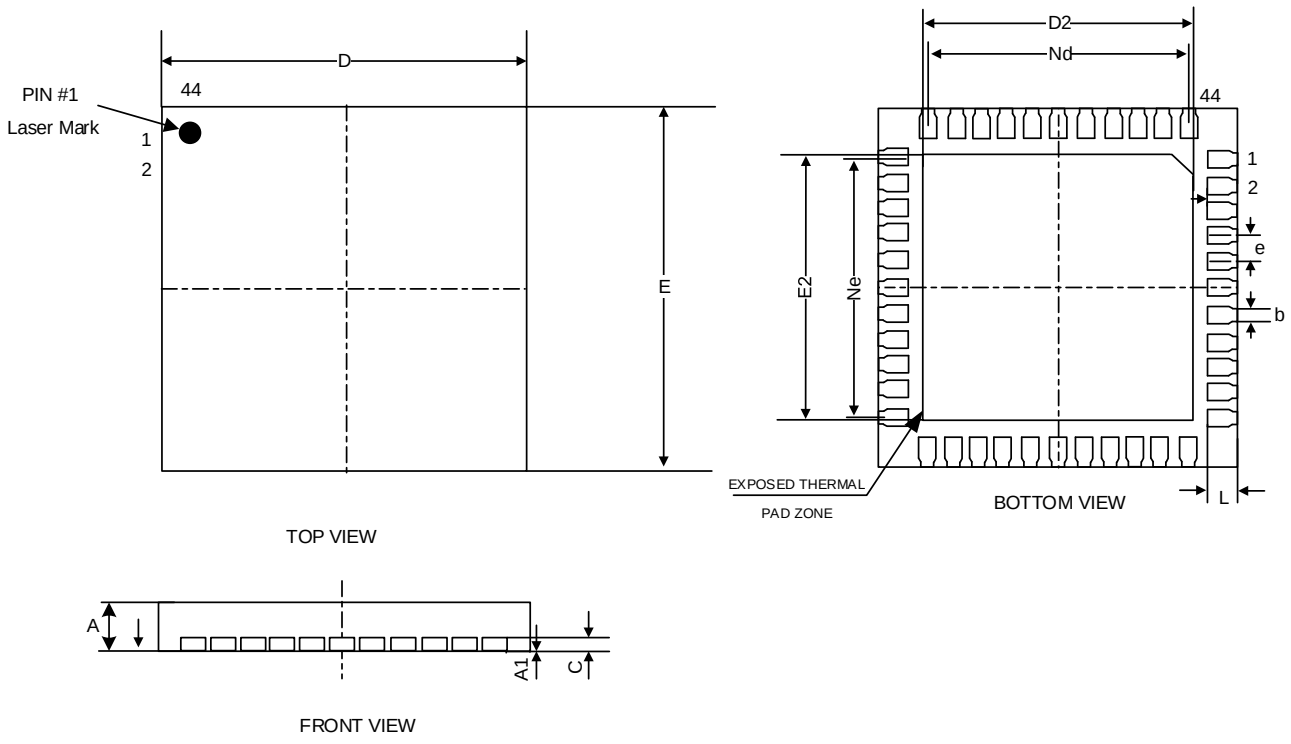


Figure 7. Schematic of GD30DR4731 Application

8 Package Information

QFN44 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 1 *QFN44 dimensions(mm)*.

Table 1 QFN44 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1		0.02	0.05
b	0.13	0.18	0.23
b1	0.05	0.10	0.15
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.50	3.60	3.70
e	0.35 BSC		
Nd	3.50BSC		
E	4.90	5.00	5.10
E2	3.50	3.60	3.70
Ne	3.50BSC		
L	0.35	0.40	0.45

9 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DR4731YUTR-K	QFN44	Green	Tape & Reel	3000	−40°C to +85°C

10 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company according to the laws of the People’s Republic of China and other applicable laws. The Company reserves all rights under such laws and no Intellectual Property Rights are transferred (either wholly or partially) or licensed by the Company (either expressly or impliedly) herein. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. Unless otherwise expressly specified in the datasheet of the Product , the Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.