32-bit High Performance Controller with Integrated 150V 3-Phase BLDC Gate Driver

1 Features

- System Core
  - Integrated 32-bit high performance and low power consumption ARM Cortex-M33
  - Integrated Nested Vectored Interrupt Controller(NVIC)
  - Up to 180 MHz operation frequency
  - 24-bit Systick timer
- Memory Map
  - Up to 512 Kbytes of flash memory
  - Up to 128 Kbytes of SRAM
- Clock Control
  - Internal 8 MHz factory-trimmed RC and external 4 to 32 MHz crystal oscillator
  - Internal 48 MHz RC oscillator
  - Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
  - Integrated system clock PLL
- Power and Reset
  - Three power domains: VDD, VDDA, VBAK and 1.71 to 3.63 V application supply and I/Os
  - Three power saving modes: sleep, deep-sleep and standby modes
  - Low voltage detector(LVD)
  - Reset as power on and power down
- Analog to Digital Converter(ADC)
  - 16 channel external analog inputs
  - 12-bit SAR ADC's conversion rate is up to 2.5 MSPS
  - 12-bit, 10-bit, 8-bit or 6-bit configurable resolution
  - Hardware oversampling ratio adjustable from 2 to 256x improves resolution to 16-bit
  - Input voltage range: V_{REF-} to V_{REF+}
- Digital to Analog Converter(DAC)
  - Three 12-bit DACs with independent output channels
  - 8-bit or 12-bit mode in conjunction with the DMA controller
- DMA
  - 7 channels for DMA0 controller and 5 channels for DMA1 controller
  - Peripherals supported: Timers, SHRTIMER, ADCs, DACs, SPIs, I2Cs, I2S and USARTs
- GPIOs
  - Up to 62 fast GPIOs, all mappable on 16 external interrupt lines
  - Analog input/output configurable
  - Alternate function input/output configurable
- Timer and PWM Generation
  - Two 16-bit advanced timer (TIMER0(Internal), TIMER7), one 32-bit general timer (TIMER1), up to twelve 16-bit general timers (TIMER2~TIMER4, TIMER8~TIMER16)
  - Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
  - 16-bit, motor control PWM advanced timer with programmable dead-time generation for output match
  - 24-bit SysTick timer down counter
  - 2 watchdog timers (free watchdog timer and window watchdog timer)
- Real Time Clock(RTC)
  - 32-bit programmable counter with a programmable 20-bit prescaler
  - Alarm function
  - Interrupt and wakeup event
- Inter-Integrated Circuit(I2C)

  I2C1:
  - Support both master and slave mode with a

frequency up to 1 MHz (Fast mode plus)
  - Provide arbitration function, optional PEC (packet error checking) generation and checking
  - Supports 7-bit and 10-bit addressing mode and general call addressing mode
  - SMBus 2.0 and PMBus compatible
  - Supports SAM_V mode

  I2C2:
  - Support both master and slave mode with a frequency up to 1 MHz (Fast mode plus)
  - Provide arbitration function, optional PEC (packet error checking) generation and checking
  - Supports 7-bit and 10-bit addressing mode and general call addressing mode
  - SMBus 3.0 and PMBus 1.3 compatible
  - Wakeup from Deep-sleep mode on address match
- Serial Peripheral Interface(SPI)
  - Up to three SPI interfaces with a frequency of up to 22.5 MHz
  - Support both master and slave mode
  - Hardware CRC calculation and transmit automatic CRC error checking
  - Quad-SPI configuration available in master mode (only in SPI0)
- USART

  USART0~2, UART3~4:
  - Maximum speed up to 22.5 MBits/s
  - Supports both asynchronous and clocked synchronous serial communication modes
  - IrDA SIR encoder and decoder support
  - LIN break generation and detection
  - ISO 7816-3 compliant smart card interface

  USART5:
  - Maximum speed up to 22.5 MBits/s
  - Supports both asynchronous and clocked synchronous serial communication modes
  - IrDA SIR encoder and decoder support
  - LIN break generation and detection
  - ISO 7816-3 compliant smart card interface
  - Dual clock domain
  - Wake up from Deep-sleep mode
- Comparators(CMP)
  - Three fast rail-to-rail low-power comparators with software configurable
  - Programmable reference voltage (internal or external I/O)
- Controller Area Network(CAN)
  - Three CAN interfaces supports the CAN protocols version 2.0A and B, ISO11891-1:2015 and BOSCH CAN FD specification with baud rates up to 1 Mbit/s when classical frames and 6 Mbit/s when FD frames
  - Supports CAN FD Frame with up to 64 data bytes (ISO11898-1 and Bosch CAN FD specification V1.0)
- Debug mode
  - Serial wire JTAG debug port (SWJ-DP)
- Motro Driver
  - High-end floating bootstrap power supply design, with a voltage withstand capability of 150V
  - Supports the highest frequency of 500KHz
  - Built-in dead-time control circuit
  - Upper and lower bridge power supply under-voltage protection, with start and protection points at 4.4V and 4.1V
  - Internally integrated low-internal-resistance bootstrap charging diode
  - Output pull and sink current Io+/Io- is +1.0A/-1.3A
  - HIN input active high, controls the upper bridge HO output
  - LIN input active high, controls the lower bridge LO output
  - Under Voltage Protection
- Package: QFN88
- RoHS Compliant and Halogen-Free

2 Applications

- Brushless DC motor control
- Permanent magnet synchronous motor control
- Servo motor control
- Robotics and RC toys
- Industrial automation

3 Description

The GD30DRE518 device integrates a 32-bit ARM® Cortex®-M33 core and a 150V three-phase gate driver. The device supports multiple applications, such as motors, electronic bikes, power tools, etc.

The device provides up to 512 KB on-chip flash memory and up to 128 KB SRAM memory. An extensive range of enhanced I/O and peripherals connected to two APB buses. The devices offer 16 channel 12-bit ADC, three 12-bit DACs with independent output channel, 7 channels for DMA0 controller and 5 channels for DMA1 controller, Up to 62 fast GPIOs, all mappable on 16 external interrupt lines, three fast rail-to-rail low power comparators with software configurable, two 16-bit advanced timer, one 32-bit general timer, up to twelve 16-bit general timers, as well as standard communication interfaces: SPI, I2C, USART, I2S.

The driver of GD30DRE518 integrated three half-bridge gate drivers, capable of driving high-side and low-side N-channel power MOSFETs. The GD30DRE518 generates the correct gate drive voltages using an integrated bootstrap diode and external capacitor for high-side MOSFETs. VCC is used to generate gate drive voltage for the low-side MOSFETs. The gate drive architecture supports peak up to 1.0A source and 1.3A sink current. The drive currents will be adapted automatically to the optimized current according to different power MOSFET used in the application.

The device inserts fixed dead-time and uses automatic handshaking to prevent the high-side and low-side MOSFETs from shoot-through when switching.

The phase pins VSx is able to tolerate the significant negative voltage transients; while high side gate driver supply VBx and HOx is able to support to higher positive voltage transients (150V) abs max voltage which improves robustness of the system. Small propagation delay and delay matching specifications minimize the dead-time requirement which further improves efficiency. Undervoltage protection is provided for both low and high side through VCC and BST undervoltage lockout.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30DRE518	QFN88	9.00 mm x 9.00 mm

1. For packaging details, see *Package Information* section.

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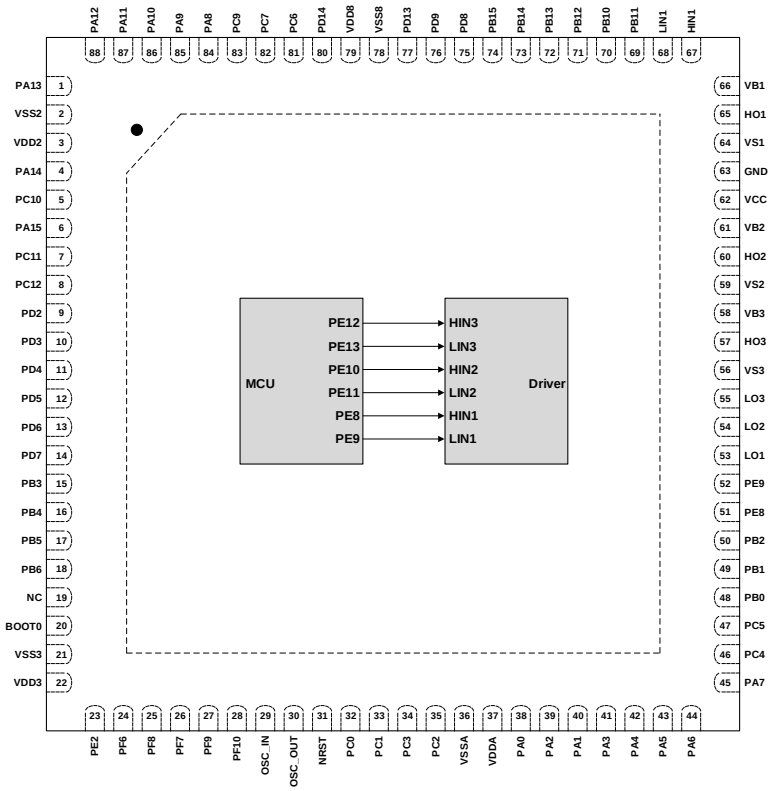
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	IO LEVEL	FUNCTION
NAME	NUM			
PA13	1	IO	5VT	Default: JTMS, SWDIO Remap: PA13
VSS2	2	G		Connect to GND.
VDD2	3	P		Power supply for digital circuit. Connect a X5R or X7R, VDD2-rated ceramic and greater then or equal to 0.1uF local capacitance between the VDD2 and VSS2 pin.
PA14	4	IO	5VT	Default: JTCK, SWCLK Remap: PA14
PC10	5	IO	5VT	Default: PC10 Alternate1: I2C2_SCL Alternate2: UART3_TX Remap: USART2_TX, SPI2_SCK, I2S2_CK
PA15	6	IO	5VT	Default: JTDI Alternate1: SHRTIMER_FLT1

PIN NUMBER		PIN TYPE[1]	IO LEVEL	FUNCTION
NAME	NUM			
				Alternate2: SPI2_NSS, I2S2_WS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS
PC11	7	IO	5VT	Default: PC11 Alternate1: SHRTIMER_EXEV1, I2S2_ADD_SD Alternate2: UART3_RX Remap: USART2_RX, SPI2_MISO
PC12	8	IO	5VT	Default: PC12 Alternate1: SHRTIMER_EXEV0 Alternate2: UART4_TX Remap: USART2_CK, SPI2_MOSI, I2S2_SD
PD2	9	IO	5VT	Default: PD2 Alternate2: TIMER2_ETI, UART4_RX
PD3	10	IO	5VT	Default: PD3 Remap: USART1_CTS
PD4	11	IO	5VT	Default: PD4 Alternate1: SHRTIMER_FLT2 Remap: USART1_RTS
PD5	12	IO	5VT	Default: PD5 Alternate1: SHRTIMER_EXEV2 Remap: USART1_TX
PD6	13	IO	5VT	Default: PD6 Remap: USART1_RX
PD7	14	IO	5VT	Default: PD7 Remap: USART1_CK
PB3	15	IO	5VT	Default: JTDO Alternate1: SHRTIMER_SCOUT, SHRTIMER_EXEV8 Alternate2: SPI2_SCK, I2S2_CK Remap: TIMER1_CH1, PB3, SPI0_SCK, TRACESWO
PB4	16	IO	5VT	Default: NJTRST Alternate1: SHRTIMER_EXEV6, I2C2_SDA, I2S2_ADD_SD, TIMER15_CH0, TIMER16_BRKIN Alternate2: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO
PB5	17	IO		Default: PB5 Alternate1: USBHS_ULPI_D7, SHRTIMER_EXEV5, I2C2_SCL, TIMER15_BRKIN, TIMER16_CH0 Alternate2: SPI2_MOSI, I2S2_SD, WKUP5, Remap: TIMER2_CH1, SPI0_MOSI, CAN1_RX
PB6	18	IO	5VT	Default: PB6 Alternate1: SHRTIMER_SCIN, SHRTIMER_EXEV3, TIMER15_CH0_ON

PIN NUMBER		PIN TYPE[1]	IO LEVEL	FUNCTION
NAME	NUM			
				Alternate2: TIMER3_CH0 Remap: USART0_TX, CAN1_TX, SPI0_IO2
NC	19			No Connection.
BOOT0	20	I		Default: BOOT0
VSS3	21	G		Connect to GND.
VDD3	22	P		Power supply for digital circuit. Connect a X5R or X7R, VDD2-rated ceramic and greater then or equal to 0.1uF local capacitance between the VDD3 and VSS3 pin.
PE2	23	IO	5VT	Default: PE2
PF6	24	IO		Default: PF6 Alternate2: ADC2_IN4 Remap: TIMER9_CH0
PF8	25	IO		Default: PF8 Alternate2: ADC2_IN6, WKUP7 Remap: TIMER12_CH0
PF7	26	IO		Default: PF7 Alternate2: ADC2_IN5 Remap: TIMER10_CH0
PF9	27	IO		Default: PF9 Alternate2: ADC2_IN7 Remap: TIMER13_CH0
PF10	28	IO		Default: PF10 Alternate2: ADC2_IN8
OSC_IN	29	I		Default: OSCIN
OSC_OUT	30	O		Default: OSCOUT
NRST	31	IO		Default: NRST
PC0	32	IO		Default: PC0 Alternate1: USBHS_ULPI_STP Alternate2: ADC012_IN10
PC1	33	IO		Default: PC1 Alternate2: ADC012_IN11
PC3	34	IO		Default: PC3 Alternate1: USBHS_ULPI_NXT Alternate2: ADC012_IN13
PC2	35	IO		Default: PC2 Alternate1: USBHS_ULPI_DIR, I2S1_ADD_SD Alternate2: ADC012_IN12, ETH_MII_TXD2
VSSA	36	G		Connect to AGND.
VDDA	37	P		Power supply for analog circuit. Connect a X5R or X7R, VDD2-rated ceramic and greater then or equal to 0.1uF local capacitance

PIN NUMBER		PIN TYPE[1]	IO LEVEL	FUNCTION
NAME	NUM			
				between the VDDA and VSSA pin.
PA0	38	IO		Default: PA0 Alternate2: WKUP0, USART1_CTS, ADC012_IN0, TIMER1_CH0, TIMER1_ETI, TIMER4_CH0, TIMER7_ETI
PA2	39	IO		Default: PA2 Alternate1: CMP1_OUT, TIMER14_CH0 Alternate2: USART1_TX, TIMER4_CH2, ADC012_IN2, TIMER8_CH0, TIMER1_CH2, SPI0_IO2, WKUP3, CMP1_IM6
PA1	40	IO		Default: PA1 Alternate1: TIMER14_CH0_ON Alternate2: USART1_RTS, ADC012_IN1, TIMER4_CH1, TIMER1_CH1
PA3	41	IO		Default: PA3 Alternate1: USBHS_ULPI_D0, TIMER14_CH1 Alternate2: USART1_RX, TIMER4_CH3, ADC012_IN3, TIMER1_CH3, TIMER8_CH1, SPI0_IO3
PA4	42	IO		Default: PA4 Alternate2: SPI0_NSS, USART1_CK, DAC_OUT0, ADC01_IN4, CMP1_IM4, CMP3_IM4, CMP5_IM4 Remap: SPI2_NSS, I2S2_WS
PA5	43	IO		Default: PA5 Alternate1: USBHS_ULPI_CK Alternate2: SPI0_SCK, ADC01_IN5, DAC_OUT1, CMP1_IM5, CMP3_IM5, CMP5_IM5
PA6	44	IO		Default: PA6 Alternate1: TIMER15_CH0 Alternate2: SPI0_MISO, TIMER7_BRKIN, ADC01_IN6, TIMER2_CH0, TIMER12_CH0, DAC1_OUT0 Remap: TIMER0_BRKIN
PA7	45	IO		Default: PA7 Alternate1: TIMER16_CH0 Alternate2: SPI0_MOSI, TIMER7_CH0_ON, ADC01_IN7, TIMER2_CH1, TIMER13_CH0, CMP1_IP Remap: TIMER0_CH0_ON
PC4	46	IO		Default: PC4 Alternate2: ADC01_IN14
PC5	47	IO		Default: PC5 Alternate1: TIMER14_BRKIN Alternate2: ADC01_IN15, WKUP4
PB0	48	IO		Default: PB0 Alternate1: USBHS_ULPI_D1

PIN NUMBER		PIN TYPE[1]	IO LEVEL	FUNCTION
NAME	NUM			
				Alternate2: ADC01_IN8, TIMER2_CH2, TIMER7_CH1_ON, CMP3_IP Remap: TIMER0_CH1_ON
PB1	49	IO		Default: PB1 Alternate1: CMP3_OUT, USBHS_ULPI_D2, SHRTIMER_SCOUT Alternate2: ADC01_IN9, TIMER2_CH3, TIMER7_CH2_ON, ETH_MII_RXD3 Remap: TIMER0_CH2_ON
PB2	50	IO	5VT	Default: PB2, BOOT1 Alternate1: USBHS_ULPI_D4, SHRTIMER_SCIN Alternate2: CMP3_IM7
PE8	51	IO	5VT	Default: PE8 Remap: TIMER0_CH0_ON
PE9	52	IO	5VT	Default: PE9 Remap: TIMER0_CH0
LO1	53	O		Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
LO2	54	O		Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
LO3	55	O		Low-side gate driver output. Connect to the gate of the low-side power MOSFET.
VS3	56	I		High-side source sense input. Connect to the high-side power MOSFET source.
HO3	57	O		High-side gate driver output. Connect to the gate of the high-side power MOSFET.
VB3	58	O		Bootstrap output pin. Connect capacitor between VB3 and VS3.
VS2	59	I		High-side source sense input. Connect to the high-side power MOSFET source.
HO2	60	O		High-side gate driver output. Connect to the gate of the high-side power MOSFET.
VB2	61	O		Bootstrap output pin. Connect capacitor between VB2 and VS2.
VCC	62	P		Gate driver power supply input. Connect a X5R or X7R, GVDD-rated ceramic and greater then or equal to 10-uF local capacitance between the GVDD and GND pins.
GND	63	G		Device ground.
VS1	64	I		High-side source sense input. Connect to the high-side power MOSFET source.
HO1	65	O		High-side gate driver output. Connect to the gate of the high-side power MOSFET.
VB1	66	O		Bootstrap output pin. Connect capacitor between VB1 and VS1.

PIN NUMBER		PIN TYPE[1]	IO LEVEL	FUNCTION
NAME	NUM			
HPE8	67	I		Must be connected to PE8.
LPE9	68	I		Must be connected to PE9.
PB11	69	IO	5VT	Default: PB11 Alternate1: CAN2_TX, USBHS_ULPI_D4, SHRTIMER_FLT3 Alternate2: I2C1_SDA, USART2_RX, CMP5_IP Remap: TIMER1_CH3
PB10	70	IO	5VT	Default: PB10 Alternate1: CAN2_RX, USBHS_ULPI_D3, SHRTIMER_FLT2 Alternate2: I2C1_SCL, USART2_TX Remap: TIMER1_CH2
PB12	71	IO	5VT	Default: PB12 Alternate1: USBHS_ULPI_D5, SHRTIMER_ST2CH0 Alternate2: SPI1_NSS, I2S1_WS, I2C1_SMBA, USART2_CK, TIMER0_BRKIN, CAN1_RX
PB13	72	IO	5VT	Default: PB13 Alternate1: USBHS_ULPI_D6, SHRTIMER_ST2CH1 Alternate2: SPI1_SCK, I2S1_CK, USART2_CTS, TIMER0_CH0_ON, CAN1_TX, I2C1_TXFRAME
PB14	73	IO	5VT	Default: PB14 Alternate1: SHRTIMER_ST3CH0, I2S1_ADD_SD, TIMER14_CH0 Alternate2: SPI1_MISO, USART2_RTS, TIMER0_CH1_ON, TIMER11_CH0
PB15	74	IO	5VT	Default: PB15 Alternate1: SHRTIMER_ST3CH1, TIMER14_CH1, TIMER14_CH0_ON Alternate2: SPI1_MOSI, TIMER0_CH2_ON, I2S1_SD, TIMER11_CH1, WKUP6, CMP5_IM7
PD8	75	IO	5VT	Default: PD8 Remap: USART2_TX
PD9	76	IO	5VT	Default: PD9 Remap: USART2_RX, ETH_MII_RXD0, ETH_RMII_RXD0
PD13	77	IO	5VT	Default: PD13 Remap: TIMER3_CH1
VSS8	78	G		Connect to GND.
VDD8	79	P		Power supply for digital circuit. Connect a X5R or X7R, VDD2-rated ceramic and greater then or equal to 0.1uF local capacitance between the VDD3 and VSS3 pin.
PD14	80	IO	5VT	Default: PD14 Remap: TIMER3_CH2
PC6	81	IO	5VT	Default: PC6 Alternate1: SHRTIMER_EXEV9, CMP5_OUT, USART5_TX

PIN NUMBER		PIN TYPE[1]	IO LEVEL	FUNCTION
NAME	NUM			
				Alternate2: I2S1_MCK, TIMER7_CH0 Remap: TIMER2_CH0
PC7	82	IO	5VT	Default: PC7 Alternate1: SHRTIMER_FLT4, USART5_RX Alternate2: I2S2_MCK, TIMER7_CH1 Remap: TIMER2_CH1
PC9	83	IO	5VT	Default: PC9 Alternate1: SHRTIMER_ST4CH1, I2C2_SDA Alternate2: TIMER7_CH3 Remap: TIMER2_CH3
PA8	84	IO	5VT	Default: PA8 Alternate1: SHRTIMER_ST0CH0, I2C2_SCL Alternate2: USART0_CK, TIMER0_CH0, CK_OUT, USBHS_SOF, CTC_SYNC
PA9	85	IO	5VT	Default: PA9 Alternate1: CAN2_RX, SHRTIMER_ST0CH1, I2C2_SMBA, TIMER14_BRKIN Alternate2: USART0_TX, TIMER0_CH1, USBHS_VBUS
PA10	86	IO	5VT	Default: PA10 Alternate1: CAN2_TX, CMP5_OUT, SHRTIMER_ST1CH0, TIMER16_BRKIN Alternate2: USART0_RX, TIMER0_CH2, USBHS_ID
PA11	87	IO		Default: PA11 Alternate1: SHRTIMER_ST1CH1, USART5_TX Alternate2: USART0_CTS, CAN0_RX, TIMER0_CH3, USBHS_DM
PA12	88	IO		efault: PA12 Alternate1: CMP1_OUT, SHRTIMER_FLT0, USART5_RX, TIMER15_ CH0 Alternate2: USART0_RTS, CAN0_TX, TIMER0_ETI, USBHS_DP
Thermal PAD	89	G		Connection the thermal pad to a large-area ground plane. The thermal pad is internally connected to GND.

1. I = input, O = Output, IO = Input and Output, P = power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1,2]

SYMBOL	PARAMETER	MIN	MAX	UNIT
Digital				
V_{DDx}	External supply voltage range[2]	V_{SS} − 0.3	V_{SS} + 3.63	V
V_{DDA}	External analog supply voltage range	V_{SS} − 0.3	V_{SS} + 3.63	V
V_{IN}	Input voltage on 5V tolerant pin[3]	V_{SS} − 0.3	V_{DD} + 3.63	V
	Input voltage on other I/O	V_{SS} − 0.3	3.63	V
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins		50	mV
$\|V_{SSX}-V_{SS}\|$	Variations between different ground pins		50	mV
I_{IO}	Maximum current for GPIO pins		±25	mA
P_D	Power dissipation at T_A = 85°C		820	mW
Analog				
V_{CC}	Gate driver regulator power supply pin voltage range	−0.3	20	V
V_{BX}	Bootstrap pin voltage	−0.3	150	V
V_{SX}	High-side source pin voltage	VB−20	VB+0.3	V
V_{HOX}	High-side gate drive output pin voltage	VS−0.3	VB+0.3	V
V_{LOX}	Low-side gate drive output pin voltage	−0.3	VCC+0.3	V
P_D	Power dissipation at T_A = 85°C		500	mW
GD30DRE518				
T_J	Maximum junction temperature		125	°C
T_A	Operating temperature range	−40	+85	°C
T_{STG}	Storage temperature range	−65	+150	°C

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.
2. Guaranteed by design, not tested in production.
3. All main power and ground pins should be connected to an external power source within the allowable range.
4. VIN maximum value cannot exceed 5.5 V.

5.2 Recommended Operation Conditions

SYMBOL[1]	PARAMETER	MIN	TYP	MAX	UNIT
Digital DC Operating Conditions[1]					
V_{DDX}	Digital supply voltage	1.62	3.3	3.63	V
V_{DDA}	Analog supply voltage, f_{ADCMAX} = 35 MHz	2.4	3.3	3.63	V
	Analog supply voltage, f_{ADCMAX} = 14 MHz	1.62		3.63	
Digital Clock Frequency[2]					
f_{HCLK}	AHB clock frequency			180	MHz
f_{APB1}	APB1 clock frequency			90	MHz
f_{APB2}	APB2 clock frequency			180	MHz
Digital Power Up/Down[2]					
t_{VDD}	V_{DD} rise time rate	0		∞	μs/ V
	V_{DD} fall time rate	50		∞	
Start Up Timing of Operating Condition[1,3,4]					
$t_{start-up}$	Start-up time, Clock source from HXTAL		2270		μs
	Start-up time, Clock source from IRC8M		104.8		
Power Saving Mode Wakeup Timings Characteristics[1,5]					
t_{Sleep}	Wakeup from Sleep mode		2.16		μs
$t_{Deep-sleep}$	Wakeup from Deep-sleep mode (LDO On)		4.74		
	Wakeup from Deep-sleep mode (LDO in low power mode)		4.74		
	Wakeup from Deep-sleep mode1 (LDO in low power and low driver mode)		7.16		
	Wakeup from Deep-sleep mode2 (LDO in low power and low driver mode)		7.84		
$t_{Standby}$	Wakeup from Standby mode		105.2		
Gate Driver Operating Conditions					
V_{CC}	Gate driver regulator supply voltage	4	15	18	V
V_{BX}	Bootstrap pin voltage		V_S+15	V_S+18	V
V_{SX}	High-side source pin voltage	−6[6]		150	V
	Transient 100ns high-side gate drive pin voltage	−36		150	
C_{BOOT}	Capacitor between VBX and VSX pin			22	nF
GD30DRE518					
T_A	Operating temperature range	−40		85	°C

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. After power-up, the start-up time is the time between the rising edge of NRST high and the first I/O instruction conversion in SystemInit function.
4. PLL is off.
5. The wakeup time is measured from the wakeup event to the point at which the application code reads the first instruction

under the below conditions: VDD = 3.3 V, IRC8M = System clock = 8 MHz.

6. Direct current negative voltage, at this time the minimum value of VB−VS is 12V.

5.3 Digital Electrical Characteristics

5.3.1 Power Supplies Supervisor Characteristics

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

SYMBOL[2,3,4,5,6]	PARAMETER	CONDITIONS	MIN	TYP[1]	MAX	UNIT
$I_{DD}+I_{DDA}$	Supply current (Run mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 180 MHz, All peripherals enabled		62.68		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 180 MHz, All peripherals disabled		23.25		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 160 MHz, All peripherals enabled		55.87		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 160 MHz, All peripherals disabled		20.78		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 120 MHz, All peripherals enabled		42.23		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 120 MHz, All peripherals disabled		15.86		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, All peripherals enabled		38.1		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 108 MHz, All peripherals disabled		14.38		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, All peripherals enabled		34.03		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 96 MHz, All peripherals disabled		12.91		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals enabled		25.82		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 72 MHz, All peripherals disabled		9.96		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals enabled		17.64		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 48 MHz, All peripherals disabled		6.98		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals enabled		13.51		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 36 MHz, All peripherals disabled		5.51		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals enabled		9.39		mA

SYMBOL[2,3,4,5,6]	PARAMETER	CONDITIONS	MIN	TYP[1]	MAX	UNIT
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 24 MHz, All peripherals disabled		4.05		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals enabled		6.63		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 16 MHz, All peripherals disabled		3.08		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals enabled		3.36		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System clock = 8 MHz, All peripherals disabled		1.61		mA
	Supply current (Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 180 MHz, CPU clock off, All peripherals enabled		49.60		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 180 MHz, CPU clock off, All peripherals disabled		9.21		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 160 MHz, CPU clock off, All peripherals enabled		44.24		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 25 MHz, System Clock = 160 MHz, CPU clock off, All peripherals disabled		8.30		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 120 MHz, CPU clock off, All peripherals enabled		33.49		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 120 MHz, CPU clock off, All peripherals disabled		6.49		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 108 MHz, CPU clock off, All peripherals enabled		30.26		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 108 MHz, CPU clock off, All peripherals disabled		5.95		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 96 MHz, CPU clock off, All peripherals enabled		27.03		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 96 MHz, CPU clock off, All peripherals disabled		5.41		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 72 MHz, CPU clock off, All		20.56		mA

SYMBOL[2,3,4,5,6]	PARAMETER	CONDITIONS	MIN	TYP[1]	MAX	UNIT
		peripherals enabled				
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 72 MHz, CPU clock off, All peripherals disabled		4.33		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 48 MHz, CPU clock off, All peripherals enabled		14.09		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 48 MHz, CPU clock off, All peripherals disabled		3.26		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 36 MHz, CPU clock off, All peripherals enabled		10.85		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 36 MHz, CPU clock off, All peripherals disabled		2.73		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 24 MHz, CPU clock off, All peripherals enabled		7.61		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 24 MHz, CPU clock off, All peripherals disabled		2.19		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 16 MHz, CPU clock off, All peripherals enabled		5.45		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 16 MHz, CPU clock off, All peripherals disabled		1.83		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 8 MHz, CPU clock off, All peripherals enabled		2.78		mA
		V_{DD} = V_{DDA} = 3.3 V, HXTAL = 8 MHz, System Clock = 8 MHz, CPU clock off, All peripherals disabled		0.99		mA
	Supply current (Deep-Sleep mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and normal driver mode, IRC40K off, RTC off		146.47		µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and normal driver mode, IRC40K off, RTC off		96.70		µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in normal power and low driver mode, IRC40K off, RTC off		106.67		µA
		V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off		59.20		µA

SYMBOL[2,3,4,5,6]	PARAMETER	CONDITIONS	MIN	TYP[1]	MAX	UNIT
	Supply current (Deep-Sleep 1 mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off		48.30		μA
	Supply current (Deep-Sleep 2 mode)	V_{DD} = V_{DDA} = 3.3 V, LDO in low power and low driver mode, IRC40K off, RTC off		30.04		μA
	Supply current (Standby mode)	V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC on		3.07		μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K on, RTC off		2.82		μA
		V_{DD} = V_{DDA} = 3.3 V, LXTAL off, IRC40K off, RTC off		2.06		μA
I_{BAT}	Battery supply current (Backup mode)	V_{DD} off, V_{DDA} off, V_{BAT} = 3.63 V, LXTAL on with external crystal, RTC on, LXTAL High driving		2.30		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL High driving		2.18		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL High driving		2.02		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL High driving		1.90		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.63 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving		1.82		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving		1.71		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving		1.55		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium High driving		1.44		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.63 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving		1.33		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving		1.23		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low driving		1.07		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Medium Low		0.96		μA

SYMBOL[2,3,4,5,6]	PARAMETER	CONDITIONS	MIN	TYP[1]	MAX	UNIT
		driving				
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.63 V, LXTAL on with external crystal, RTC on, LXTAL Low driving		1.18		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 3.3 V, LXTAL on with external crystal, RTC on, LXTAL Low driving		1.07		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 2.5 V, LXTAL on with external crystal, RTC on, LXTAL Low driving		0.92		μA
		V_{DD} off, V_{DDA} off, V_{BAT} = 1.8 V, LXTAL on with external crystal, RTC on, LXTAL Low driving		0.81		μA

1. Based on characterization, not tested in production.
2. Unless otherwise specified, all values given for T_A = 25°C and test result is mean value.
3. When System Clock is less than 4 MHz, an external source is used, and the HXTAL bypass function is needed, no PLL.
4. When System Clock is greater than 8 MHz, a crystal 8 MHz is used, and the HXTAL bypass function is closed, using PLL.
5. When analog peripheral blocks such as ADCs, DACs, HXTAL, LXTAL, IRC8M, or IRC40K are ON, an additional power consumption should be considered.
6. All GPIOs are configured as analog mode except standby mode.

5.3.2 External Clock Characteristics

Table 1. High Speed External Clock (HXTAL) Generated from a Crystal/Ceramic Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{HXTAL}[1]	Crystal or ceramic frequency	1.71 V ≤ V_{DD} ≤ 3.63 V	4	8	32	MHz
R_F[2]	Feedback resistor	V_{DD} = 3.3 V		400		kΩ
C_{HXTAL}[2,3]	Recommended load capacitance on OSCIN and OSCOUT			20	30	pF
$Ducy_{(HXTAL)}$[2]	Crystal or ceramic duty cycle		30	50	70	%
g_m[2]	Oscillator transconductance	Startup		20		mA/V
$I_{DDHXTAL}$[1]	Crystal or ceramic operating current	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz		0.38		mA
$t_{SUHXTAL}$[1]	Crystal or ceramic startup time	V_{DD} = 3.3 V, f_{HCLK} = f_{IRC8M} = 8 MHz		2		ms

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. C_{HXTAL1} = C_{HXTAL2} = 2*(C_{LOAD} - C_S), For C_{HXTAL1} and C_{HXTAL2}, it is recommended matching capacitance on OSCIN and OSCOUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.

Table 2. High speed external clock characteristics (HXTAL in bypass mode)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{HXTAL_ext}[1]	External clock source or oscillator frequency	1.71 V ≤ V_{DD} ≤ 3.63 V	1		50	MHz
V_{HXTALH}[2]	OSCIN input pin high level voltage	V_{DD} = 3.3 V	0.7V_{DD}		V_{DD}	V
V_{HXTALL}[2]	OSCIN input pin low level voltage		V_{SS}		0.3V_{DD}	V
$t_{H/L(HXTAL)}$[2]	OSCIN high or low time		5			ns
$t_{R/F(HXTAL)}$[2]	OSCIN rise or fall time				10	ns
C_{IN}[2]	OSCIN input capacitance			5		pF
$Ducy_{(HXTAL)}$[2]	Duty cycle		40		60	%

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 3. Low Speed External Clock (LXTAL) Generated from a Crystal/Ceramic Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{LXTAL}[1]	Crystal or ceramic frequency	V_{DD} = 3.3 V		32.768		kHz
C_{LXTAL}[2,3]	Recommended matching capacitance on OSC32IN and OSC32OUT			10		pF
$Ducy_{(LXTAL)}$[2]	Crystal or ceramic duty cycle		30		70	%
g_m[2]	Oscillator transconductance	Lower driving capability		4		μA/V
		Medium low driving capability		6		
		Medium high driving capability		16		
		Higher driving capability		20		
$I_{DDLXTAL}$(1)	Crystal or ceramic operating current	LXTALDRI[1:0] = 00		0.8		μA
		LXTALDRI[1:0] = 01		1.0		
		LXTALDRI[1:0] = 10		1.4		
		LXTALDRI[1:0] = 11		2.0		
$t_{SULXTAL}$[1,4]	Crystal or ceramic startup time			0.6		s

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. C_{LXTAL1} = C_{LXTAL2} = 2*(C_{LOAD} - C_S), For C_{LXTAL1} and C_{LXTAL2}, it is recommended matching capacitance on SC32IN and OSC32OUT. For C_{LOAD}, it is crystal/ceramic load capacitance, provided by the crystal or ceramic manufacturer. For C_S, it is PCB and MCU pin stray capacitance.
4. $t_{SULXTAL}$ is the startup time measured from the moment it is enabled (by software) to the 32.768 kHz oscillator stabilization flags is SET. This value varies significantly with the crystal manufacturer.

Table 4. Low Speed External User Clock Characteristics (LXTAL in bypass mode)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{LXTAL_ext}[1]	External clock source or oscillator frequency	V_{DD} = 3.3 V		32.768	1000	kHz
V_{LXTALH}[2]	OSC32IN input pin high level voltage		0.7V_{DD}		V_{DD}	V
V_{LXTALL}[2]	OSC32IN input pin low level voltage		V_{SS}		0.3V_{DD}	
$t_{H/L(LXTAL)}$[2]	OSC32IN high or low time		450			ns
$t_{R/F(LXTAL)}$[2]	OSC32IN rise or fall time				50	
C_{IN}[2]	OSC32IN input capacitance			5		pF
$Ducy_{(LXTAL)}$[2]	Duty cycle		30	50	70	%

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.3 Internal Clock Characteristics

Table 5. High Speed Internal Clock (IRC8M) Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{IRC8M}	High Speed Internal Oscillator (IRC8M) frequency	V_{DD} = V_{DDA} = 3.3 V		8		MHz
ACC_{IRC8M}	IRC8M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = −40 °C to +85 °C[1]	−2.5		+2.5	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C to +85 °C[1]	−2		+2	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 25 °C	−1.0		+1.0	%
	IRC8M oscillator Frequency accuracy, User trimming step(1)			0.5		%
$Ducy_{IRC8M}$[2]	IRC8M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC8M}$[1]	IRC8M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V		48		μA
$t_{SUIRC8M}$[1]	IRC8M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V		1.65		μs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 6. Low Speed Internal Clock (IRC40K) Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{IRC40K}[1]	Low Speed Internal oscillator (IRC40K) frequency	V_{DD} = V_{DDA} = 3.3 V, T_A = −40 °C to +85 °C	31	40	53	kHz
$I_{DDAIRC40K}$[2]	IRC40K oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz		0.4		μA
$t_{SUIRC40K}$[2]	IRC40K oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz		1.3		μs

1. Based on characterization, not tested in production.

2. Guaranteed by design, not tested in production.

Table 7. High Speed Internal Clock (IRC48M) Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{IRC48M}	High Speed Internal Oscillator (IRC48M) frequency	V_{DD} = 3.3 V		48		MHz
ACC_{IRC48M}	IRC48M oscillator Frequency accuracy, Factory-trimmed	V_{DD} = V_{DDA} = 3.3 V, T_A = −40 °C to +85 °C(1)	−2.5		+2.5	%
		V_{DD} = V_{DDA} = 3.3 V, T_A = 0 °C to +85 °C (1)	−2.5		+2.0	%
		V_{DD} = V_{DDA} = 3.3 V	−1.0		+1.0	%
	IRC48M oscillator Frequency accuracy, User trimming step(1)			0.13		%
D_{IRC48M}[2]	IRC48M oscillator duty cycle	V_{DD} = V_{DDA} = 3.3 V	45	50	55	%
$I_{DDAIRC48M}$[1]	IRC48M oscillator operating current	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz		270		µA
$t_{SUIRC48M}$[1]	IRC48M oscillator startup time	V_{DD} = V_{DDA} = 3.3 V, f_{HCLK} = f_{HXTAL_PLL} = 180 MHz		1.3		µs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.4 PLL Characteristics

Table 8. PLL Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{PLLIN}[1]	PLL input clock frequency		2		16	MHz
f_{PLLOUT}[2]	PLL output clock frequency		16		180	MHz
f_{VCO}[2]	PLL VCO output clock frequency		32		360	MHz
t_{LOCK}[2]	PLL lock time				300	µs
I_{DDA}[1,3]	Current consumption on V_{DDA}	VCO freq = 360 MHz		700		µA
I_{DD}[1,3]	Current consumption on V_{DD}	VCO freq = 360 MHz		500		µA
$Jitter_{PLL}$[1,4]	Cycle to cycle Jitter(rms)	System clock		30		ps
	Cycle to cycle Jitter (peak to peak)			600		

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. System clock = IRC8M = 8 MHz, PLL clock source = IRC8M/2 = 4 MHz, f_{PLLOUT} = 180 MHz.
4. Value given with main PLL running.

Table 9. PLL1 Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{PLLIN}[1]	PLL input clock frequency		2		16	MHz
f_{PLLOUT}[2]	PLL output clock frequency		16		100	MHz
f_{VCO}[2]	PLL VCO output clock frequency		32		180	MHz
t_{LOCK}[2]	PLL lock time				300	μs
I_{DDA}[1]	Current consumption on V_{DDA}	VCO freq = 180 MHz		400		μA
I_{DD}[1]	Current consumption on V_{DD}	VCO freq = 180 MHz		250		μA
$Jitter_{PLL}$[1]	Cycle to cycle Jitter			40		ps

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 10. PLL2 Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{PLLIN}[1]	PLL input clock frequency		2		16	MHz
f_{PLLOUT}[2]	PLL output clock frequency		16		200	MHz
f_{VCO}[2]	PLL VCO output clock frequency		32		360	MHz
t_{LOCK}[2]	PLL lock time				300	μs
I_{DDA}[1]	Current consumption on V_{DDA}	VCO freq = 360 MHz		700		μA
I_{DD}[1]	Current consumption on V_{DD}	VCO freq = 360 MHz		500		μA
$Jitter_{PLL}$[1]	Cycle to cycle Jitter			30		ps

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 11. PLLUSB Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}[1]	PLL input clock frequency		4		30	MHz
f_{PLLOUT}[2]	PLL output clock frequency			480		MHz
t_{LOCK}[2]	PLL lock time			100	150	μs
$Jitter_{PLL}$[1]	Cycle to cycle Jitter	System clock		40		ps
	Cycle to cycle Jitter (peak to peak)			400		

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 12. PLL Spread Spectrum Clock Generation (SSCG) Characteristics[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{mod}	Modulation frequency				10	KHz
mdamp	Peak modulation amplitude				2	%
MODCNT* MODSTEP					$2^{15}-1$	

1. Guaranteed by design, not tested in production.

SSCG configuration equation:

$$MODCNT = round(f_{PLLIN} / 4 / f_{mod}) \quad (1)$$

$$MODSTEP = round(mdamp * PLLIN * 2^{15} / (MODCNT * 100)) \quad (2)$$

5.3.5 Memory Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN[1]	TYP[1]	MAX	UNIT
PE_{CYC}	Number of guaranteed program /erase cycles before failure (Endurance)	T_A = −40 °C to +85 °C	100			kcycles
t_{RET}	Data retention time	T_A = −40 °C to +85 °C	10			years
t_{PROG}	Word programming time	T_A = −40 °C to +85 °C		20		μs
t_{ERASE}	Page erase time	T_A = −40 °C to +85 °C	1		20	ms
t_{MERASE}	Mass erase time	T_A = −40 °C to +85 °C		20		ms

1. Based on characterization, not tested in production.

5.3.6 NRST Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IL(NRST)}$[1]	NRST Input low level voltage	V_{DD} = V_{DDA} = 1.71 V			0.35V_{DD}	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		0.65V_{DD}			
V_{hyst}[1]	Schmidt trigger Voltage hysteresis			300		mV
$V_{IL(NRST)}$[1]	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.3 V			0.35V_{DD}	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		0.65V_{DD}			
V_{hyst}[1]	Schmidt trigger Voltage hysteresis			390		mV
$V_{IL(NRST)}$[1]	NRST Input low level voltage	V_{DD} = V_{DDA} = 3.63 V			0.35V_{DD}	V
$V_{IH(NRST)}$[1]	NRST Input high level voltage		0.65V_{DD}			
V_{hyst}[1]	Schmidt trigger Voltage hysteresis			400		mV
R_{pu}[2]	Pull-up equivalent resistor			40		kΩ

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

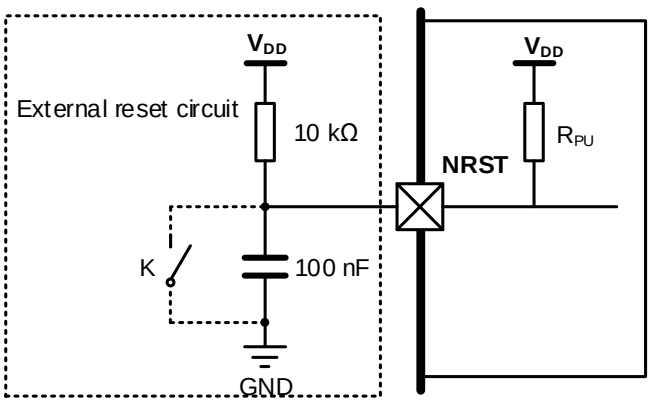


Figure 1. Recommended External NRST Pin Circuit

1. Unless the voltage on NRST pin go below VIL(NRST) level, the device would not generate a reliable reset.

5.3.7 GPIO Characteristics

Table 13. I/O Port DC Characteristics[1]

SYMBOL	PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	Standard IO Low level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V			0.35V_{DD}	V
	5V-tolerant IO Low level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V			0.35V_{DD}	V
V_{IH}	Standard IO High level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V	0.65V_{DD}			V
	5V-tolerant IO High level input voltage		1.71 V ≤ V_{DD} = V_{DDA} ≤ 3.63 V	0.65V_{DD}			V
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 1.71V			0.22	V
			V_{DD} = 3.3 V			0.13	
			V_{DD} = 3.63V			0.13	
V_{OL}	Low level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 1.71V			0.77	V
			V_{DD} = 3.3 V			0.34	
			V_{DD} = 3.63V			0.33	
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +8 mA)		V_{DD} = 1.71V	1.42			V
			V_{DD} = 3.3 V	3.14			
			V_{DD} = 3.63V	3.48			
V_{OH}	High level output voltage for an IO Pin (I_{IO} = +20 mA)		V_{DD} = 1.71V				V
			V_{DD} = 3.3 V	2.88			
			V_{DD} = 3.63V	3.24			
R_{PU}[2]	Internal pull-up resistor	All pins			40		kΩ
		PA10			10		
R_{PD}[2]	Internal pull-down resistor	All pins			40		kΩ
		PA10			10		

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 14. I/O Port AC Characteristics[1,2]

GPIOx_MDy[1:0] bit value(3)	PARAMETER	CONDITIONS	MAX	UNIT
GPIOx_CTL->MDy[1:0]=10 (IO_Speed = 2MHz)	Maximum frequency[4]	1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	2.7	MHz
		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	2.3	
		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	2	
GPIOx_CTL->MDy[1:0] = 01 (IO_Speed = 10MHz)	Maximum frequency[4]	1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	14.8	MHz
		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	12.7	
		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	11.2	
GPIOx_CTL->MDy[1:0]=11 (IO_Speed = 50MHz)	Maximum frequency[4]	1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	34.5	MHz
		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	26.3	
		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	23.2	
GPIOx_CTL->MDy[1:0]=11 and	Maximum frequency[4]	1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 10 pF	145	MHz

GPIOx_MDy[1:0] bit value(3)	PARAMETER	CONDITIONS	MAX	UNIT
GPIOx_SPDy=1 (IO_Speed = MAX)		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 30 pF	114	
		1.8 ≤ V_{DD} ≤ 3.63 V, C_L = 50 pF	86	

1. Based on characterization, not tested in production.
2. Unless otherwise specified, all test results given for T_A = 25°C.
3. The I/O speed is configured using the GPIOx_CTL -> MDy[1:0] bits. Refer to the GD32E51x user manual which is selected to set the GPIO port output speed.
4. The maximum frequency is defined in Figure 2, and maximum frequency cannot exceed 180 MHz.

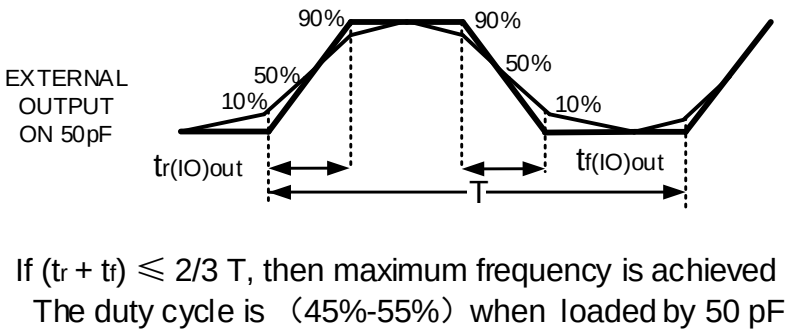


Figure 2. I/O Port AC Characteristics Defintion

5.3.8 ADC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDA}(1)	Operating voltage		1.62	3.3	3.63	V
V_{IN}(1)	ADC input voltage range		0		V_{REFP}	V
V_{REFP}(2)(3)	Positive Reference Voltage		1.62		V_{DDA}	V
V_{REFN}(2)	Negative Reference Voltage			V_{SSA}		V
f_{ADC}(1)	ADC clock	V_{DDA} = 1.62 V to 2.4 V	0.1		14	MHz
		V_{DDA} = 2.4 V to 3.63 V	0.1		35	MHz
f_S(1)	Sampling rate	12-bit	0.007		2.5	MSPS
		10-bit	0.008		2.92	
		8-bit	0.01		3.5	
		6-bit	0.013		4.38	
V_{AIN}(1)	Analog input voltage	16 external; 2 internal	0		V_{DDA}	V
R_{AIN}(2)	External input impedance	See Equation(2)			175.8	kΩ
R_{ADC}(2)	Input sampling switch resistance				0.5	kΩ
C_{ADC}(2)	Input sampling capacitance	No pin/pad capacitance included			4	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 35 MHz		15.94	497.77	μs
t_s(2)	Sampling time	f_{ADC} = 35 MHz	0.043		6.84	μs
t_{CONV}(2)	Total conversion time(including sampling time)	12-bit		14		1 / f_{ADC}
		10-bit		12		
		8-bit		10		

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
		6-bit		8		
t_{SU}(2)	Startup time				1	μs

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. V_{REFP} should always be equal to or less than V_{DDA}, especially during power up.

R_{AIN} max formula

$$R_{AIN} < \frac{T_S}{f_{ADC} * C_{ADC} * \ln(2^{N+2})} - R_{ADC} \quad (3)$$

The formula above Equation(3) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 15. ADC R_{AIN} Max for f_{ADC} = 35MHz

T_s (CYCLES)	t_s (μs)	$R_{AIN\ max}$ (kΩ)
1.5	0.043	0.6
7.5	0.21	5.0
13.5	0.39	9.4
28.5	0.81	20.5
41.5	1.19	30.0
55.5	1.59	40.0
71.5	2.04	52.0
239.5	6.84	175.8

Table 16. ADC Dynamic Accuracy at f_{ADC} = 14MHz V_{DDA} = 1.8V[1]

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f_{ADC} = 14 MHz V_{DDA} = V_{REFP} = 1.8 V Input Frequency = 20 kHz	Single ended	10.6	10.8		bits
			Differential	11	11.2		
SNDR	Signal-to-noise and distortion ratio		Single ended	65	66.5		dB
			Differential	68.3	68.9		
SNR	Signal-to-noise ratio		Single ended	65.8	67.07		
			Differential	69.2	69.7		
THD	Total harmonic distortion		Single ended		-74.4	-73.9	
			Differential		-81	-75	

1. Based on characterization, not tested in production.

Table 17. ADC Dynamic Accuracy at f_{ADC} = 35MHz V_{DDA} = 3.3V[1]

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f_{ADC} = 35 MHz V_{DDA} = V_{REFP} =3.3 V Input Frequency = 20 kHz	Single ended	10.7	11.1		bits
			Differential	11	11.3		
SNDR	Signal-to-noise and distortion ratio		Single ended	66.5	67.7		dB
			Differential	67.4	70		
SNR	Signal-to-noise ratio		Single ended	67.4	68.7		
			Differential	68	71		
THD	Total harmonic		Single ended		−74	−73	

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
	distortion		Differential		−81	−75	

1. Based on characterization, not tested in production.

Table 18. ADC Dynamic Accuracy at f_{ADC} = 35MHz V_{DDA} = 2.4V[1]

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
ENOB	Effective number of bits	f_{ADC} = 35 MHz V_{DDA} = V_{REFP} =2.4 V Input Frequency = 20 kHz	Single ended	10.7	10.9		bits
			Differential	11.1	11.3		
SNDR	Signal-to-noise and distortion ratio		Single ended	66	67.5		dB
			Differential	68.5	70		
SNR	Signal-to-noise ratio		Single ended	67	68.5		
			Differential	68.8	71		
THD	Total harmonic distortion		Single ended		−74	−73	
			Differential		−80	−74	

1. Based on characterization, not tested in production.

Table 19. ADC Static Accuracy at f_{ADC} = 14MHz V_{DDA} = 1.8V[1]

SYMBOL	PARAMETER	CONDITIONS		TYP	MAX	UNIT
Offset	Offset error	f_{ADC} = 14 MHz V_{DDA} = V_{REFP} = 1.8 V	Single ended	±0.5	±1.5	LSB
			Differential	±0.5	±1.3	
DNL	Differential linearity error		Single ended	±0.8	±1	
			Differential	±0.3	±1	
INL	Integral linearity error		Single ended	±1	±1.5	
			Differential	±0.9	±1.2	

1. Based on characterization, not tested in production.

Table 20. ADC Static Accuracy at f_{ADC} = 35MHz V_{DDA} = 3.3V[1]

SYMBOL	PARAMETER	CONDITIONS		TYP	MAX	UNIT
Offset	Offset error	f_{ADC} = 35 MHz V_{DDA} = V_{REFP} = 3.3 V	Single ended	±1	±1.5	LSB
			Differential	±0.5	±1.5	
DNL	Differential linearity error		Single ended	±0.4	±1	
			Differential	±0.3	±1	
INL	Integral linearity error		Single ended	±0.9	±1.5	
			Differential	±0.9	±1.5	

1. Based on characterization, not tested in production.

Table 21. ADC Static Accuracy at f_{ADC} = 35MHz V_{DDA} = 2.4V[1]

SYMBOL	PARAMETER	CONDITIONS		TYP	MAX	UNIT
Offset	Offset error	f_{ADC} = 35 MHz V_{DDA} = V_{REFP} = 2.4 V	Single ended	±2	±3	LSB
			Differential	±1	±1.5	
DNL	Differential linearity error		Single ended	±0.4	±1	
			Differential	±0.3	±1	
INL	Integral linearity error		Single ended	±0.5	±1.6	
			Differential	±0.9	±1.2	

1. Based on characterization, not tested in production.

5.3.9 DAC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DDA}[1]	Operating voltage		1.8	3.3	3.63	V
V_{REFP}[2]	Positive Reference Voltage		1.8		V_{DDA}	V
V_{REFN}[2]	Negative Reference Voltage			V_{SSA}		V
R_{LOAD}[2]	Load resistance	Resistive load with buffer ON	5			kΩ
Ro[2]	Impedance output with buffer OFF				15	kΩ
C_{LOAD}[2]	Load capacitance	No pin/pad capacitance included			50	pF
DAC_OUT min[2]	Lower DAC_OUT voltage with buffer ON		0.2			V
DAC_OUT max[2]	Higher DAC_OUT voltage with buffer ON				VDDA-0.2	V
DAC_OUT min[2]	Lower DAC_OUT voltage with buffer OFF			0.5		mV
DAC_OUT max[2]	Higher DAC_OUT voltage with buffer OFF				VREF-1LSB	V
I_{DDA}[1]	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V		360		uA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V		400		uA
$I_{DDVREF+}$[1]	DAC current consumption in quiescent mode	With no load, middle code(0x800) on the input, V_{REF+} = 3.6 V		125		uA
		With no load, worst code(0xF1C) on the input, V_{REF+} = 3.6 V		330		uA
DNL[1]	Differential non-linearity error	DAC in 12-bit mode		±6		LSB
INL[1]	Integral non-linearity	DAC in 12-bit mode		±7		LSB
Offset[1]	Offset error	DAC in 12-bit mode		±18		LSB
GE[1]	Gain error	DAC in 12-bit mode			0.5	%
$T_{setting}$[1]	Settling time	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ			0.5	μs
T_{wakeup}[2]	Wakeup from off state				5	μs
Update rate[2]	Max frequency for a correct DAC_OUT change from code i to i±1LSBs	$C_{LOAD} \leq 50$ pF, $R_{LOAD} \geq 5$ kΩ			4	MS/s
PSRR[2]	Power supply rejection ratio (to V_{DDA})		50	80		dB

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.

5.3.10 Comparators Characteristics

SYMBOL[1]	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{SU}	Setup Time			5.5		μs
V_{OS}	Offset Voltage			2		mV
t_D	Propagation delay	V_{STEP} = 200 mV		28		ns
		Full Range		32		
I_{VDD}	Current consumption			360		μA
I_{LEAK}	Leakage Current			1		nA

1. Guaranteed by design, not tested in production.

5.3.11 Trigonometric Math Unit Characteristics

The TMU unit has 9 different operation modes.

Table 22. TMU Supported Instructions Characteristics[1]

MODE NUMBER	OPERATION	CYCLES
0	R0 =x * 2π	4
1	R0 = x/2π	4
2	R0 = $\sqrt{x}$	7
3	R0 =sin (x)	7
4	R0 = cos (x)	7
5	R0 = arctan (x)	7
6	R0 = Ratio of X & Y, R1 = Quadrant value (0.0, ±0.25, ±0.5)	7
7	R0 = x/y	7
8	R0 = $\sqrt{x^2+y^2}$	7

1. Guaranteed by design, not tested in production.

5.3.12 I2C Characteristics

SYMBOL[1,2,3]	PARAMETER	CONDITIONS	STANDARD MODE		Fast mode FAST MODE		FAST MODE PLUS		Unit
			Min	Max	Min	Max	Min	Max	
$t_{SCL(H)}$	SCL clock high time		4.0		0.6		0.2		μs
$t_{SCL(L)}$	SCL clock low time		4.7		1.3		0.5		μs
$t_{su(SDA)}$	SDA setup time		250		100		50		ns
$t_{h(SDA)}$	SDA data hold time		0[3]	3450	0	900	0	450	ns
$t_{r(SDA/SCL)}$	SDA and SCL rise time			1000		300		120	ns
$t_{f(SDA/SCL)}$	SDA and SCL fall time			300		300		120	ns
$t_{h(STA)}$	Start condition hold time		4.0		0.6		0.26		μs

1. Guaranteed by design, not tested in production.
2. To ensure the standard mode I2C frequency, f_{PCLK1} must be at least 2 MHz, To ensure the fast mode I2C frequency, f_{PCLK1} must be at least 4 MHz. To ensure the fast mode plus I2C frequency, f_{PCLK1} must be at least a multiple of 10 MHz.

3. The device should provide a data hold time of 300 ns at least in order to bridge the undefined region of the falling edge of SCL.

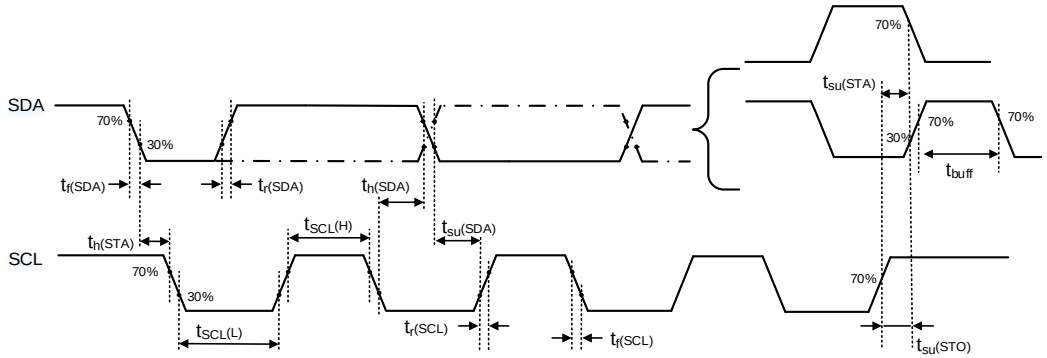


Figure 3. I2C Buc Timing Diagram

Table 23. I2C Analog Filter Delay Characteristics[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{AF}	Analog filter delay time		50	80	130	ns

1. Guaranteed by design, not tested in production.

5.3.13 SPI Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCK}	SCK clock frequency				22.5	MHz
$t_{SCK(H)}$	SCK clock high time	Master mode, f_{PCLKx} = 90 MHz, presc = 4		22.2		ns
$t_{SCK(L)}$	SCK clock low time	Master mode, f_{PCLKx} = 90 MHz, presc = 4		22.2		ns
SPI MASTER MODE						
$t_{V(MO)}$	Data output valid time				10	ns
$t_{SU(MI)}$	Data input setup time		1			ns
$t_{H(MI)}$	Data input hold time		0			ns
SPI SLAVE MODE						
$t_{SU(NSS)}$	NSS enable setup time		0			ns
$t_{H(NSS)}$	NSS enable hold time		1			ns
$t_{A(SO)}$	Data output access time			10		ns
$t_{DIS(SO)}$	Data output disable time			11		ns
$t_{V(SO)}$	Data output valid time			11		ns
$t_{SU(SI)}$	Data input setup time		0			ns
$t_{H(SI)}$	Data input hold time		1			ns

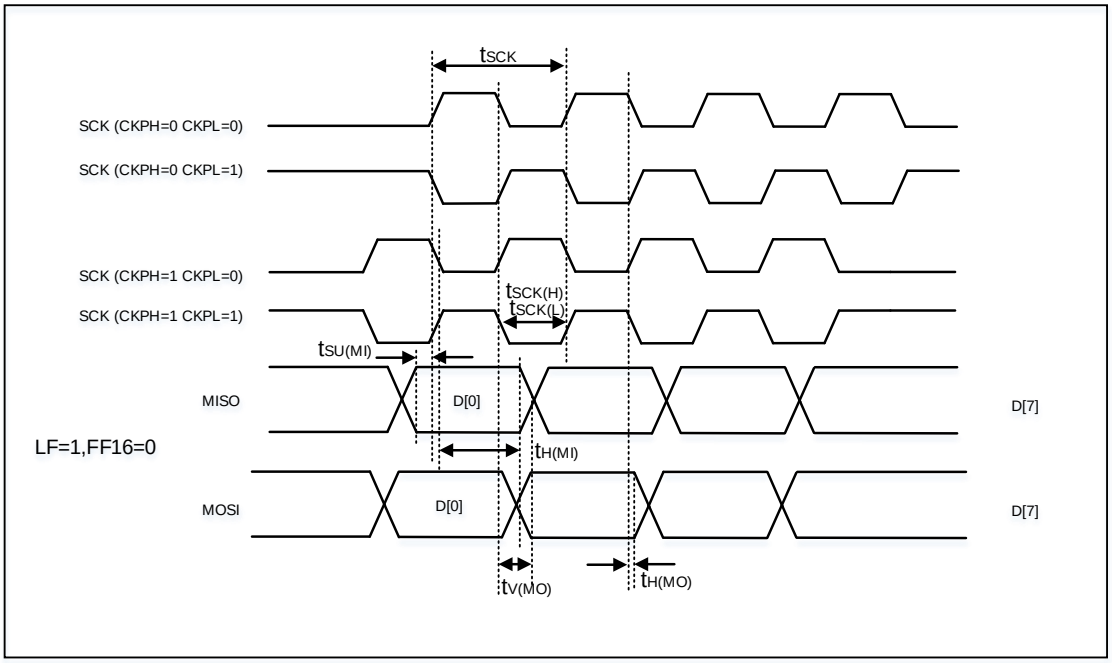


Figure 4. SPI Timing Diagram-Master Mode

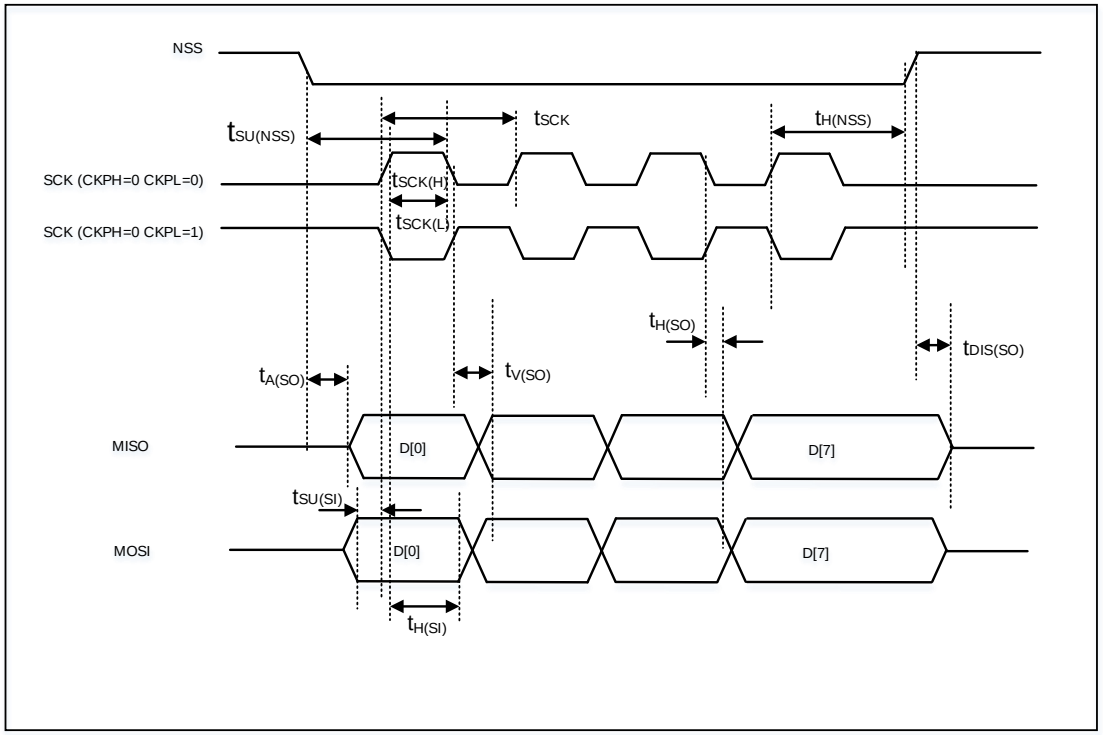


Figure 5. SPI Timing Diagram-Slave Mode

5.3.14 I2S Characteristics

SYMBOL[1,2]	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{CK}	Clock frequency	Master mode (data: 32 bits, Audio frequency = 96 kHz)		6.21		MHz
		Slave mode			12.5	
t_H	Clock high time			81		ns
t_L	Clock low time			81		ns
$t_{V(WS)}$	WS valid time	Master mode		3		ns
$t_{H(WS)}$	WS hold time	Master mode		3		ns
$t_{SU(WS)}$	WS setup time	Slave mode	0			ns
$t_{H(WS)}$	WS hold time	Slave mode	2			ns
$Ducy_{(SCK)}$	I2S slave input clock duty cycle	Slave mode		50		%
$t_{SU(SD\_MR)}$	Data input setup time	Master mode	1			ns
$t_{SU(SD\_SR)}$	Data input setup time	Slave mode	0			ns
$t_{H(SD\_MR)}$	Data input hold time	Master receiver	0			ns
$t_{H(SD\_SR)}$		Slave receiver	1			ns
$t_{V(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)			10	ns
$t_{H(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	3			ns
$t_{V(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)			10	ns
$t_{H(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0			ns

1. Guaranteed by design, not tested in production.
2. Based on characterization, not tested in production

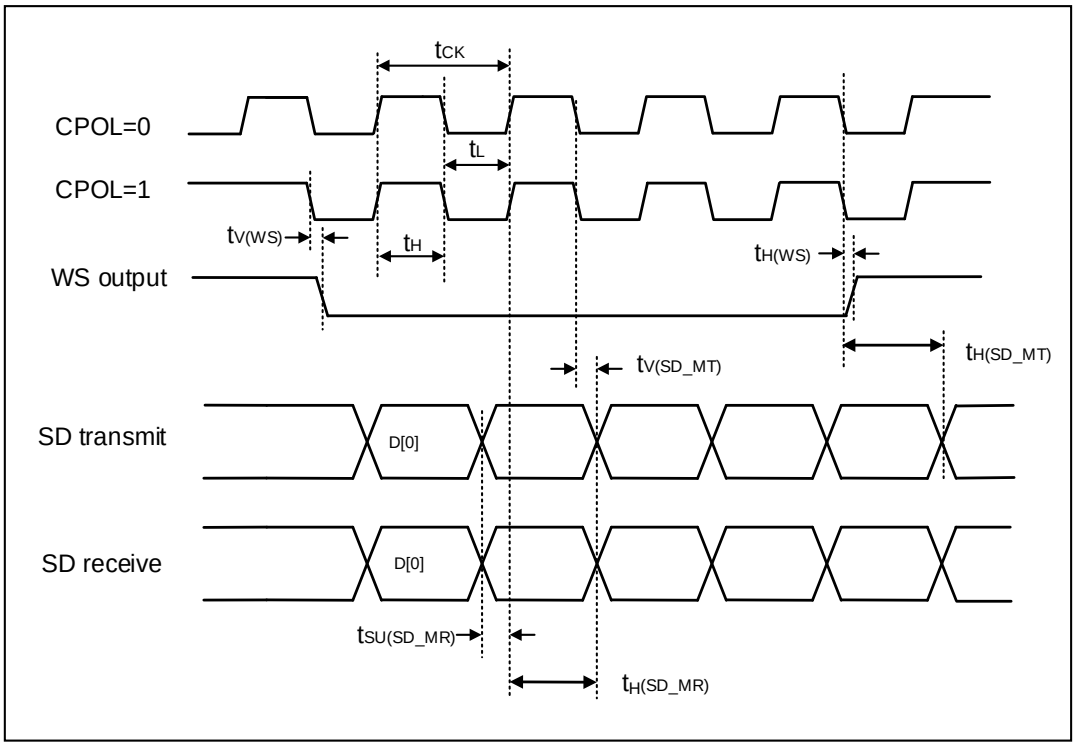


Figure 6. I2S Timing Diagram-Master Mode

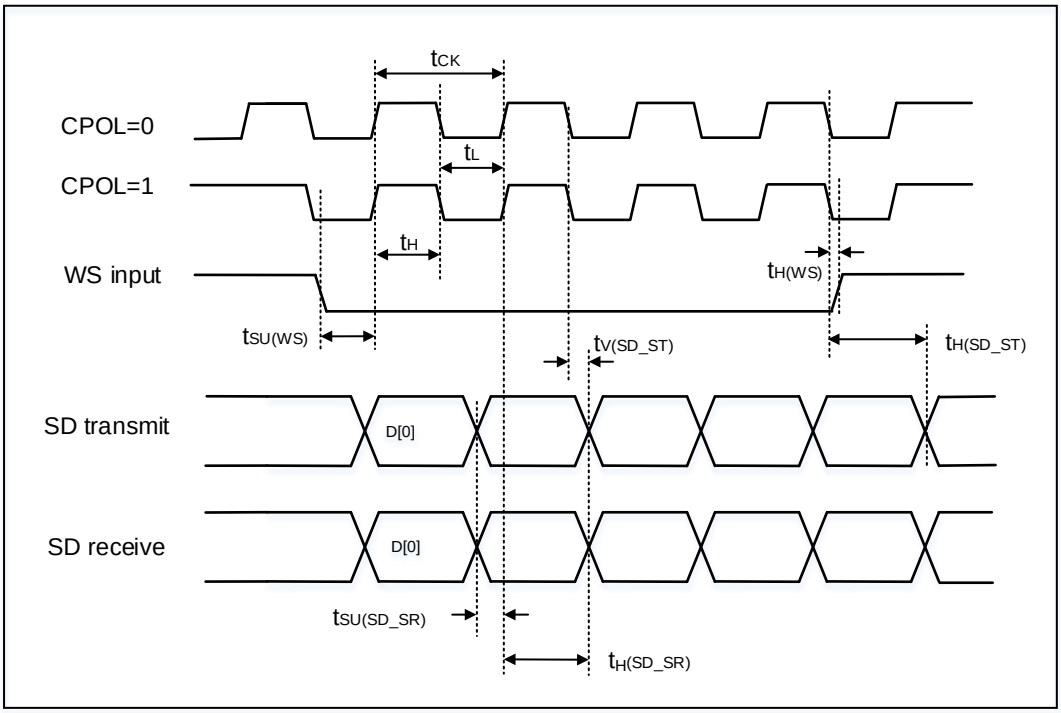


Figure 7. I2S Timing Diagram-Slave Mode

5.3.15 UART Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCK}	SCK clock frequency	f_{PCLKx} = 180 MHz			90	MHz
$t_{SCK(H)}$	SCK clock high time	f_{PCLKx} = 180 MHz	5			ns
$t_{SCK(L)}$	SCK clock low time	f_{PCLKx} = 180 MHz	5			ns

1. Guaranteed by design, not tested in production.

5.3.16 USBHS Characteristics

SYMBOL		PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD [2]		USB operating voltage		3		3.6	V
LS/FS FUNCTIONALITY							
Input levels[1]	V_{DIFS}	Differential input sensitivity(FS/LS)		0.2			V
	V_{CMFS}	Differential common mode range(FS/LS)	Includes V_{DI} range	0.8		2.5	
	V_{ILSE}	Single ended receiver low level input voltage (FS/LS)				0.8	
	V_{IHSE}	Single ended receiver high level input voltage (FS/LS)		2.0			
Output levels [2]	V_{OLFS}	Static output level low(FS/LS)	R_L of 1.0 kΩ to 3.63 V			0.3	V
	V_{OHFS}	Static output level high(FS/LS)	R_L of 15 kΩ to V_{SS}	2.8	3.3	3.6	
R_{PD}[2]		PA11, PA12(USBHS_DM/DP)	V_{IN} = V_{DD}	17	21	25	kΩ
		PA9(USBHS_VBUS)		0.72	0.9	1.1	
R_{PU}[2]		PA11, PA12(USBHS_DM/DP)	V_{IN} = V_{SS}	1.2	1.5	1.8	
		PA9(USBHS_VBUS)		0.24	0.3	0.36	
Z_{HSDRV}[1]		Driver Output Impedance	Steady state drive	40.5	45	49.5	Ω
HS FUNCTIONALITY							
Input levels[1]	V_{DIHS}	Differential input sensitivity(HS)		0.1			V
	V_{CMHS}	Differential common mode range(HS)		-50		500	mV
	V_{HSSQ}	HS Squelch Detection Threshold		100		150	mV
	V_{HSDSC}	HS Disconnect Threshold		525		625	mV
Output levels[1]	V_{OLHS}	High speed low level output voltage	45Ω load	−10		10	mV
	V_{OHHS}	High speed high level output voltage	45Ω load	360	400	440	mV

1. Guaranteed by design, not tested in production.
2. Based on characterization, not tested in production.

Table 24. USBHS Dynamic Characteristics[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{FR}	Rise time(FS/LS)	C_L = 50 pF	4	5	20	ns
T_{HSR}	Differential Rise Time(HS)		500	600		ps
T_{FF}	Fall time(FS/LS)	C_L = 50 pF	4	5	20	ns
T_{HSF}	Differential Fall Time(HS)		500	600		ps
t_{RFM}	Rise/ fall time matching(FS/LS)	t_R / t_F	90		110	%
V_{CRS}	Output signal crossover voltage(FS/LS)		1.3		2.0	V

1. Guaranteed by design, not tested in production.

Table 25. USBHS Charger Detection Characteristics[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DAT_SRC}	Data Source Voltage		0.5		0.7	V
I_{DP_SRC}	Data Connect Current		7		13	uA
V_{DAT_REF}	Data Detect Voltage		0.25		0.4	V

1. Guaranteed by design, not tested in production.

Table 26. USBHS Clock Timing Characteristics[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{DD}	USBHS operating voltage	3.0		3.6	V
f_{HCLK}	f_{HCLK} value to guarantee proper operation of USBHS interface	30			MHz
F_{START_8BIT}	Frequency (first transition) 8-bit ± 10%	54	60	66	MHz
F_{STEADY}	Frequency (steady state) ±500 ppm	59.97	60	60.63	MHz
D_{START_8BIT}	Duty cycle (first transition) 8-bit ± 10%	40	50	60	%
D_{STEADY}	Duty cycle (steady state) ±500 ppm	49.975	50	50.025	%

1. Guaranteed by design, not tested in production.

Table 27. USB-ULPI Dynamic Characteristics[1]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
t_{SC}	Control in (ULPI_DIR, ULPI_NXT) setup time			2	ns
t_{HC}	Control in (ULPI_DIR, ULPI_NXT) hold time	0.5			ns
t_{SD}	Data in setup time			2	ns
t_{HD}	Data in hold time	0			ns

1. Guaranteed by design, not tested in production.

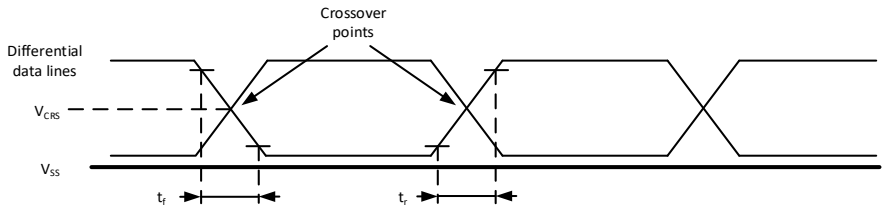


Figure 8. USBFS Timings: Definition of Data Signal Rise and Fall Time

5.3.17 CAN Characteristics

Refer to 5.3.7 *GPIO Characteristics* for more details on the input/output alternate function characteristics (CANTX and CANRX).

5.3.18 Serial/Quad Parallel Interface (SQPI) Characteristics

SYMBOL[1]	PARAMETER	MIN	TYP	MAX	UNIT
t_{CLK}[2]	CLK period	11.0[4]			ns
t_{CD}[2]	CLK high level duty for even clock divided	45	50	55	%
	CLK high level duty for odd clock divided	45		71	
t_{KHKL}[3]	CLK rise or fall time			3	ns
t_{CPH}[2]	CE# high between subsequent burst operations	22.2			ns
t_{CEM}[2]	CE# low pulse width	88.8			ns
t_{CSP}[2]	CE# setup time to CLK rising edge	5.5		177.7	ns
t_{CHD}[2]	CE# hold time from CLK rising edge	5.5		177.7	ns
t_{SP}[2]	Setup time to active CLK edge	5.5		177.7	ns
t_{HD}[2]	Hold time from active CLK edge	5.5		177.7	ns
t_{HZ}[2]	CE# rise to data output high-Z		0		ns
t_{ACLK}[2]	CLK fall to data output valid delay		0		ns
t_{KOH}[2]	Data hold time from CLK falling edge		0		ns

1. Based on characterization, not tested in production.
2. Guaranteed by design, not tested in production.
3. Output driven mode is 50 MHz. Measured from 10% to 90% of VDD.
4. This is designed minimal period. The operating minimal clock period is 22.2 ns(45 MHz = 180 MHz/4).

5.3.19 Super High-Resolution Timer (SHRTIMER) Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_A	Timer ambient temperature range	$f_{SHRTIMER}$ = 180 MHz	−40		85	°C
$f_{SHRTIMER}$	SHRTIMER input clock for DLL	Under T_A conditions		180		MHz
$t_{SHRTIMER}$				5.56		ns
$t_{res(SHRTIMER)}$	Timer resolution time	f_{HPMER} = 180 MHz		86.8		ps
$RES_{SHRTIMER}$	Timer resolution				16	bit
t_{DTG}	Dead time generator clock period		1/64		16	$t_{SHRTIMER}$
		$f_{SHRTIMER}$ = 180 MHz	0.0868		88.89	ns
$\|t_{DTR}\|$ / $\|t_{DTF}\|$	Dead time range (absolute value)				2^16-1	t_{DTG}
		$f_{SHRTIMER}$ = 180 MHz			5825.41	µs
f_{CHPFRQ}	Chopper stage clock frequency		1/256		1/16	$f_{SHRTIMER}$
		$f_{SHRTIMER}$ = 180 MHz	0.703		11.25	MHz
t_{1STPW}	Chopper first pulse length		16		256	$t_{SHRTIMER}$
		$f_{SHRTIMER}$ = 180 MHz	0.089		1.42	µs

1. Guaranteed by design, not tested in production.

Table 28. SHRTIMER Output Response to Fault Protection[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX[2]	UNIT
$t_{LAT(DF)}$	Digital fault response latency	Propagation delay from SHRTIMER_FLTx digital input to SHRTIMER_STxCHy output pin			25	ns
$t_{W(FLT)}$	Minimum fault pulse width		11			
$t_{LAT(AF)}$	Analog fault response latency	Propagation delay from comparator CMPx_IPx input to SHRTIMER_STxCHy output pin			35	

1. Guaranteed by design, not tested in production.
2. Based on characterization, not tested in production.

Table 29. SHRTIMER Output Response to External 1 to 10 (Synchronous Mode)[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX[2]	UNIT
$T_{PROP(SHRTIMER)}$	External event response latency in SHRTIMER	SHRTIMER internal propagation delay[3]	5		6	$t_{SHRTIMER}$[2]
$t_{LAT(DEEV)}$	Digital external event response latency	Propagation delay from SHRTIMER_EXEVx digital input to SHRTIMER_STxCHy output pin(30pF load) [3]			48	ns
$t_{W(FLT)}$	Minimum external event pulse width		11			
$t_{LAT(AEEV)}$	Analog external event response latency	Propagation delay from comparator CMPx_IPx input pin to SHRTIMER_STxCHy output pin(30pF load) [3]			60	
$T_{JIT(EEV)}$	External event response jitter	Jitter of the delay from SHRTIMER_EXEVx digital input or CMPx_IPx input pin to SHRTIMER_STxCHy output pin(30pF load)			1	$t_{SHRTIMER}$[2]
$T_{JIT(PW)}$	Jitter on output pulse width in response to an external event				0	$t_{SHRTIMER}$[2]

1. Guaranteed by design, not tested in production.
2. Based on characterization, not tested in production.
3. $t_{SHRTIMER}$ = 1 / $f_{SHRTIMER}$ with $f_{SHRTIMER}$ = 180 MHz depending on the clock controller configuration.
4. This parameter does not take into account latency introduced by GPIO or comparator.

Table 30. SHRTIMER Synchronization Input/Output[1]

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX[2]	UNIT
$t_{W(SYNCIN)}$	Minimum pulse width on SYNCIN inputs, including SHRTIMER_SCIN		2			$t_{SHRTIMER}$
$t_{LAT(DF)}$	Response time to external synchronization request				1	$t_{SHRTIMER}$
$t_{W(AF)}$	Pulse width on SHRTIMER_SCOUT output			16		$t_{SHRTIMER}$
		$f_{SHRTIMER}$ = 180 MHz		88.89		ns

1. Guaranteed by design, not tested in production.
2. Based on characterization, not tested in production.

5.3.20 TIMER Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
t_{res}	Timer resolution time		1		$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	5.6		ns
f_{EXT}	Timer external clock frequency		0	$f_{TIMERxCLK}/2$	MHz
		$f_{TIMERxCLK}$ = 180 MHz	0	90	MHz
RES	Timer resolution	TIMERx (except TIMER1)		16	bit
		TIMER1		32	
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected		1	65536	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	0.0056	364.1	µ6
	32-bit counter clock period when internal clock is selected (only TIMER1)		1	2^{32}	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz	0.0056	23.86	S
t_{MAX_COUNT}	Maximum possible count (except TIMER1)			$2^{16} \times 2^{16}$	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz		23.86	s
	Maximum possible count (only TIMER1)			$2^{16} \times 2^{32}$	$t_{TIMERxCLK}$
		$f_{TIMERxCLK}$ = 180 MHz		$2^{16} \times 23.86$	s

1. Guaranteed by design, not tested in production.

5.3.21 WDGT Characteristics

Prescaler divider	PSC[2:0] bits	Min timeout RLD[11:0] = 0x000	Max timeout RLD[11:0] = 0xFFF	Unit
1/4	000	0.025	409.525	ms
1/8	001	0.025	819.025	
1/16	010	0.025	1638.025	
1/32	011	0.025	3276.025	
1/64	100	0.025	6552.025	
1/128	101	0.025	13104.025	
1/256	110 or 111	0.025	26208.025	

1. Guaranteed by design, not tested in production.

Prescaler divider	PSC[1:0]	Min timeout value CNT[6:0] = 0x40	Unit	Max timeout value CNT[6:0] = 0x7F	Unit
1/1	00	45.51	µs	2.91	ms
1/2	01	91.02		5.83	
1/4	10	182.04		11.65	
1/8	11	364.08		23.30	

1. Guaranteed by design, not tested in production.

5.4 Analog Electrical Characteristics

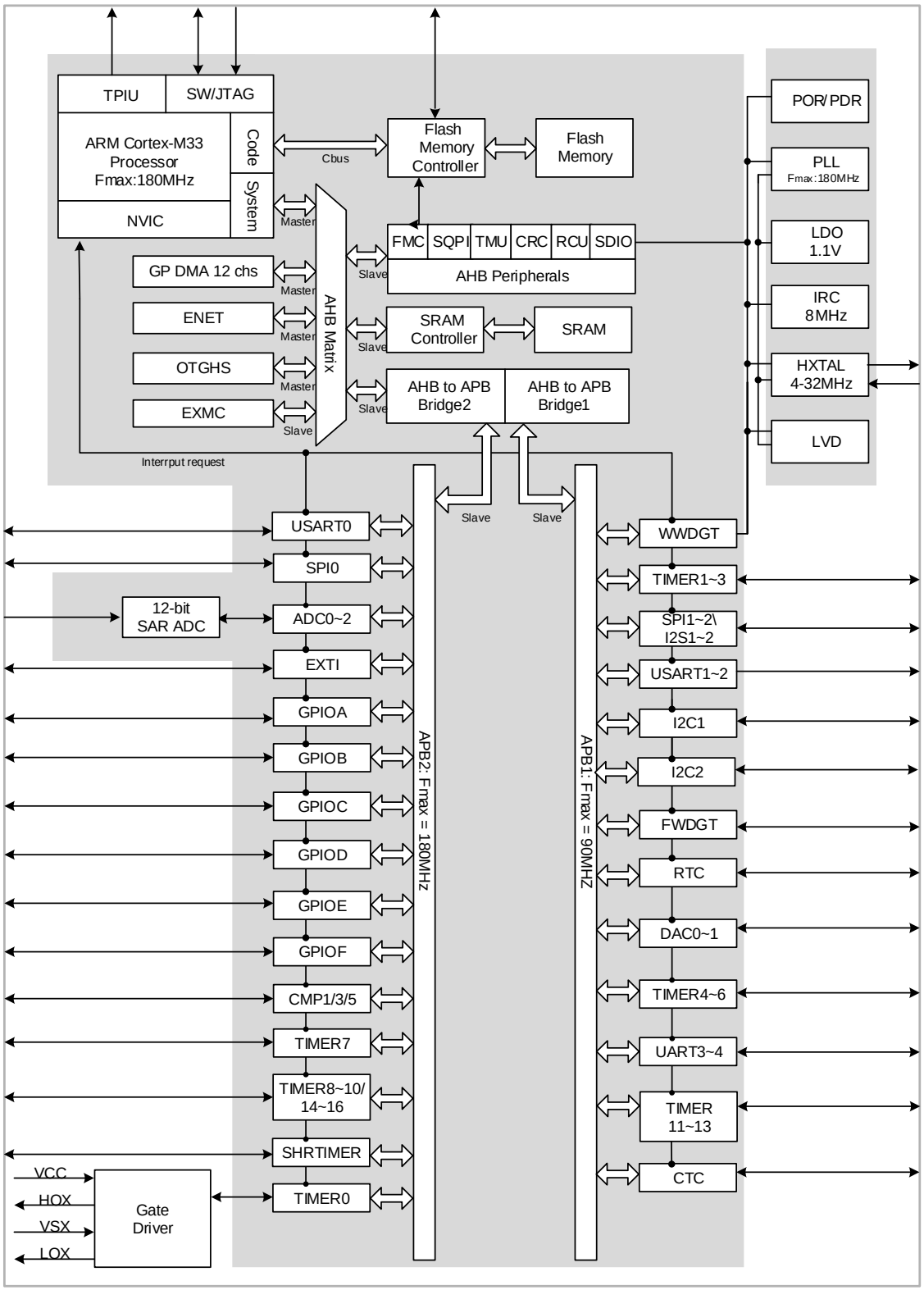
V_{CC} = 15V, VB1,2,3 = 15V, VS1,2,3 = 0V, T_A = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Static Parameters						
V_{HOHX}	High-side output high level voltage	V_{HOHX} – VB， Io+ = 10mA			100	mV
V_{HOLX}	High-side output low level voltage	V_{HOLX} – VB， Io- = 10mA			50	mV
V_{LOHX}	Low-side output high level voltage	V_{LOHX} – VCC， Io+ = 10mA			100	mV
V_{LOLX}	Low-side output low level voltage	V_{LOLX} – GND， Io- = 10mA			50	mV
I_{O+}	Output source current	Vo = 0V, V_{IN} = V_{IH}, PW≤10µs		1.0		A
I_{O-}	Output sink current	Vo = 15V, V_{IN} = V_{IL}, PW≤10µs		1.3		A
R_{BSD}	Bootstrap resistance	VCC = 15V, VB = 0V		40		Ω
I_{QCC}	Quiescent current	LIN1,2,3 = 0V		90		µA
		LIN1,2,3 = 5V		250		µA
I_{QBSX}	High-side Quiescent current	HIN1,2,3 = 0V		30		µA
		HIN1,2,3 = 5V		120		µA
V_{CCUV+}	VCC undervoltage lockout voltage			4.4		V
V_{CCUV-}				4.1		V
V_{BSUV+}	VB undervoltage lockout voltage			4.4		V
V_{BSUV-}				4.1		V
Dynamic Parameters1						
High-Side Output(HO) Switch Timing Characteristics						
t_{on}	Rise propagation time			200		ns
t_{off}	Fall propagation time			100		ns
t_r	Rise time			35		ns
t_f	Fall time			15		ns
Low-Side Output(LO) Switch Timing Characteristics						
t_{on}	Rise propagation time			200		ns
t_{off}	Fall propagation time			100		ns

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Rise time			35		ns
t_f	Fall time			15		ns
Dead Time Characteristics						
DT	Dead time			100		ns
MT	Rise time - Fall time			10		ns

6 Functional Description

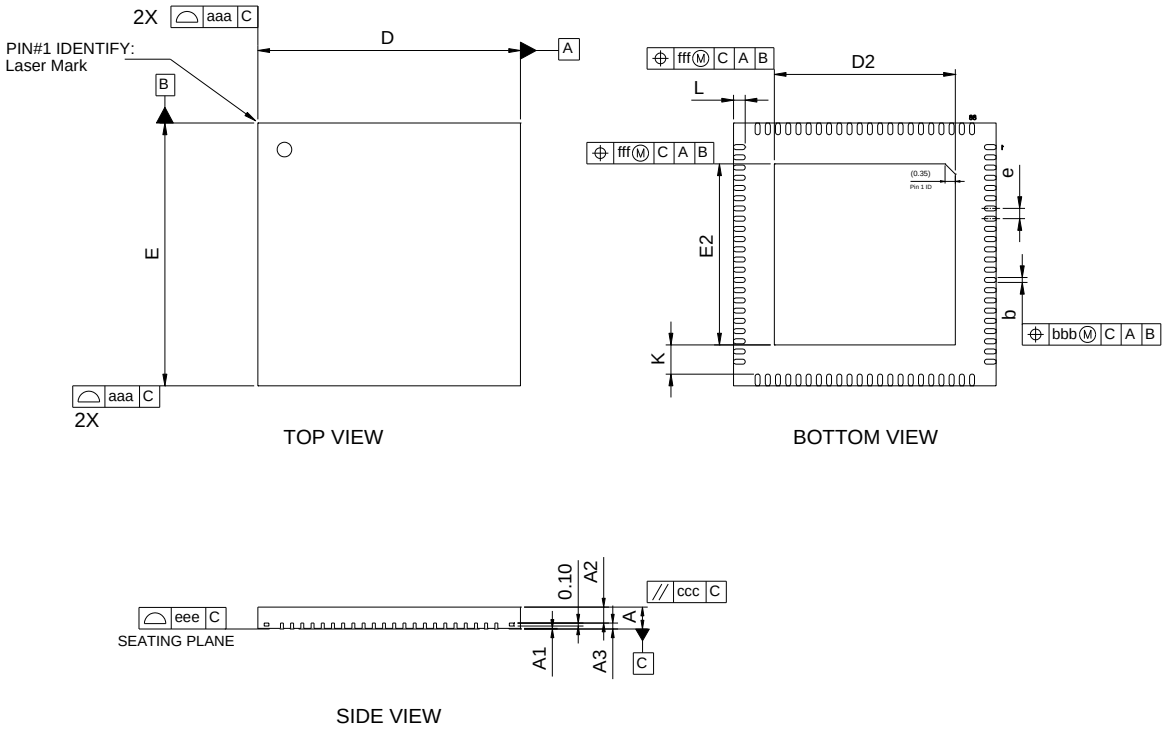
6.1 Block Diagram



7 Package Information

7.1 Outline Dimensions

QFN88 Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 31 *QFN88 dimensions(mm)*.

Table 31. QFN88 dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2		0.55	
A3	0.20 REF		
b	0.12	0.17	0.22
D	8.90	9.00	9.10
E	8.90	9.00	9.10
D2	6.10	6.20	6.30
E2	6.10	6.20	6.30
L	0.30	0.40	0.50
e	0.35 BSC		
K	1.00 REF		
aaa	0.10		
bbb	0.70		
ccc	0.10		
eee	0.08		
fff	0.10		

8 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30DRE518QUTR-K	QFN88	Green	Tape & Reel	3000	−40°C to +85°C

9 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial Release and device details	2024
1.1	Add a description of the CAN bus	2025

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