DDR5 Client VR on DIMM PMIC

1 Features

- VIN_Bulk Input Supply Range: 4.25V to 5.5V
- Three Buck Converters: SWA, SWB & SWC
- Configurable Dual Phase and Single Phase Node for SWA and SWB
- 0.75% Output Accuracy
- Configurable Switching Frequency of Buck
- CCS COT Mode Enables Fast Transient Response
- 2 LDO Regulators: VOUT_1.8V, VOUT_1.0V
- Secure Mode and Programmable Mode of Operation
- Supports I^2C and I^3C Interface
- Controllable Soft-start /Soft-stop Time of Buck
- Protection Functions, Including OVP, UVP, OCP and OTP
- Power Good Indicator
- General Status Interrupt Function
- WQFN-28 Package
- RoHS Compliant

2 Applications

- DDR5 SO-DIMM, UDIMM

3 Description

The GD30MP1020 is an integrated solution for DDR5 SODIMM and UDIMM power management IC. The PMIC features three buck converters and two LDO regulators. The buck converters are designed by capacitor current sense constant on time (CCS COT) control that provides fast transient response, the noise immunity and all kinds of very low ESR output capacitor for ensuring performance stabilization. All three buck converters equip with automatic power saving mode (PSM) for optimizing efficiency. The two LDO regulators, VOUT_1.0V and VOUT_1.8V, can supply DIMM module's sideband and SDP usage. The PMIC supports selectable interface (I2C or I3C Basic) to fit various application environment.

Two of the buck converters (SWA and SWB) can be configured to operate in dual-phase single channel. Two ADCs are implemented to monitor the current consumptions of the buck converters and the voltage information of the input/output rails.

The GD30MP1020 is available in low-profile thermal enhanced WQFN-28 (3.00 mmx4.00 mm) package.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30MP1020	WQFN-28L	3.00 mm x 4.00 mm

1. For packaging details, see *Package Information* section.

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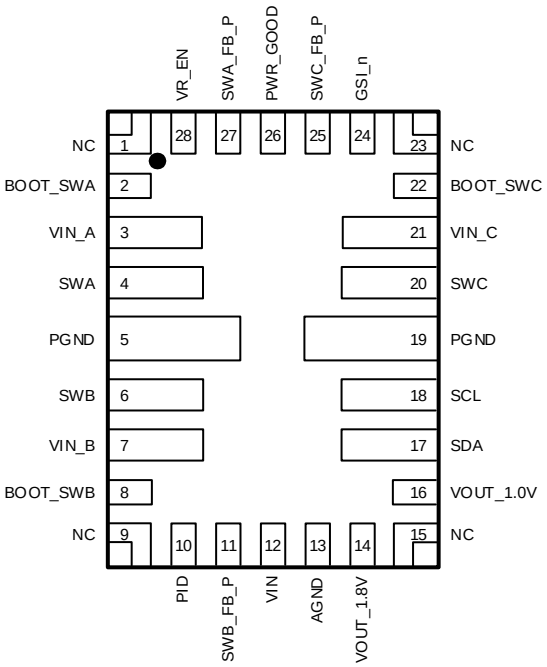
4 Device Overview

4.1 Pinout and Pin Assignment



4.2 Pin Description

PIN		PIN TYPE[1]	FUNCTION
NAME	NO		
NC	1, 9, 15, 23		Non-functional pins. No internal connections to the chip.
BOOT_SWA	2	O	Buck A bootstrap. Bootstrap node for switch node SWA high-side NMOS driver. Connect a capacitor between SWA and BOOT_SWA to form a floating supply across the high-side switch driver of Buck A.
VIN_ A VIN_ B VIN_C	3, 7, 21	P	5V power input supply to the PMIC for SWA, SWB and SWC respectively. All three VIN_Bulk input pins must be connected to the 5 V input supply even if one or more output regulators are not intended to be used.
SWA	4	P	Switch node A output buck regulator. This pin connects to L1 power inductor. In single phase regulator mode of operation, the SWA output must not be connected to SWB output even if they are configured to same exact output voltage. In dual phase regulator mode of operation, the SWA and SWB outputs are connected.
PGND	5, 19	G	Power Ground. Connect PGND to DIMM ground plane.

PIN		PIN TYPE[1]	FUNCTION
NAME	NO		
SWB	6	P	Switch node B output buck regulator. This pin connects to L2 power inductor. In single phase regulator mode of operation, the SWB output must not be connected to SWA output even if they are configured to same exact output voltage. In dual phase regulator mode of operation, the SWA and SWB outputs are connected.
BOOT_SWB	8	O	Buck B bootstrap. Bootstrap node for switch node SWB high-side NMOS driver. Connect a capacitor between SWB and BOOT_SWB to form a floating supply across the high-side switch driver of Buck B.
PID	10	I	PMIC ID pin for I^2C and I^3C Basic bus.
SWB_FB_P	11	I	Switch node B output buck regulator positive feedback. In single phase regulator mode of operation, this pin connects to DIMM power plane load. In dual phase regulator mode of operation, this pin is connected to GND.
VIN	12	P	5 V power input supply to the PMIC for analog circuits.
AGND	13	G	Analog Ground. Connect AGND to DIMM ground plane.
VLDO_1.8V	14	P	1.8V LDO Output.
VLDO_1.0V	16	P	1.0V LDO Output.
SDA	17	IO	Data input and output for I^2C and I^3C Basic bus management interface.
SCL	18	IO	Clock input for I^2C and I^3C Basic bus management interface.
SWC	20	P	Switch node C output buck regulator. This pin connects to L3 power inductor.
BOOT_SWC	22	O	Buck C bootstrap. Bootstrap node for switch node SWC high-side NMOS driver. Connect a capacitor between SWC and BOOT_SWC to form a floating supply across the high-side switch driver of Buck C.
GSI_n	24	O	General Status Interrupt. Open Drain Output. This PMIC asserts this pin low to communicate any or more events to host. This pin stays asserted until the appropriate registers are explicitly cleared and event is no longer present.
SWC_FB_P	25	P	Switch node C output buck regulator positive feedback. This pin connects to DIMM power plane load.

PIN		PIN TYPE[1]	FUNCTION
NAME	NO		
PWR_GOOD	26	O	Power good indicator. Open Drain output. The PMIC floats this pin high when VIN_Bulk input supply as well as all enabled output buck regulators and all LDO regulator tolerance threshold is maintained as configured in appropriate register. The PMIC drives this pin low when VIN_Bulk input goes below the threshold or when any of the enabled switch output regulators exceeds the threshold configured in the appropriate register or any LDO output regulator exceeds the threshold tolerance. Input: The PMIC disables its output regulators when this pin is low. The LDO outputs shall remain on.
SWA_FB_P	27	P	Switch node A output buck regulator positive feedback. In single phase or dual phase regulator mode of operation, this pin connects to DIMM power plane load.
VR_EN	28	I	PMIC Enable. When this pin is high, the PMIC turns on the regulator. When this pin is low, the PMIC turns off the regulator. This pin shall not be left floating. If it is not used, it shall be tied to GND.

1. I = Input, O = Output, IO = Input/Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}, V_{INA}, V_{INB}, V_{INC}	Supply Input Voltage	−0.3	6.0	V
AGND to PGND		−0.3	0.3	V
Other I/O		−0.3	6.0	V
SWA, SWB, SWC	DC	−0.3	6	V
	<25ns Transient	−0.3	9	V
T_J	Operating junction temperature	−40	155	°C
T_{stg}	Storage temperature	−55	150	°C
P_{max}	Maximum power dissipation @ T_A=+25°C		TBD	W

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}, V_{INA}, V_{INB}, V_{INC}	Supply Input voltage	4.25		5.5	V
T_A	Operating ambient temperature	0		85	°C
T_J	Operating junction temperature	−10		125	°C

1. The device is not guaranteed to function outside of its operating conditions.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	WQFN28	TBD	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	WQFN28	TBD	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

Limits apply over the full operating ambient temperature range (0°C ≤ T_A ≤ +85°C) and V_{INA} = V_{INB} = V_{INC} = V_{IN} = 5V, typical values are at T_A=+25°C, unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Power Supply						
V_{IN}	Input Supply Voltage DC Voltage		4.25	5	5.5	V
V_{INA}, V_{INB}, V_{INC}	Input supply Voltage VINA, VINB, VINC	V_{IN} Rising	4.25	5	5.5	V
I_{Q_VIN}	VIN Supply Current	VR_EN=0; all LDO, SWA to SWC off, T_A=25°C			25	μA
SWA / SWB						
$V_{OUT\_SWA/B}$	Output Voltage Setting	Setting by reg_0x21[7:1]/ 0x25[7:1]	0.8	1.1	1.435	V
$V_{OUT\_SWA/B}$	Output Voltage Accuracy	V_{BAT}=5V only, I_{out}=0, CCM	−0.75		0.75	%
	Dynamic Voltage Scale slew rate			1		mV/μs
	Soft-start Time	t_{set}= 1ms to 14 ms	−15		15	%
	Soft-stop Time	t_{set}= 0.5ms to 4 ms	−20		20	%
$R_{DS(ON)\_SWA/SWB\_H}$	High side MOSFET $R_{DS(ON)}$			16		mΩ
$R_{DS(ON)\_SWA/SWB\_L}$	Low side MOSFET $R_{DS(ON)}$			10		mΩ
$f_{SW\_SWA/B}$	Switching Frequency	Setting by reg_0x29[5:4]/ 0x2A[5:4]=00 (default)	−15%	0.75	+15%	MHz
		Setting by reg_0x29[5:4]/ 0x2A[5:4]=01	−15%	1.0	+15%	
		Setting by reg_0x29[5:4]/ 0x2A[5:4]=10	−15%	1.25	+15%	
		Setting by reg_0x29[5:4]/ 0x2A[5:4]=11	−15%	1.5	+15%	
	OVP Threshold	Setting by reg_0x22[5:4]/ 0x26[5:4]=00		7.5		%
		Setting by reg_0x22[5:4]/ 0x26[5:4]=01		10		
		Setting by reg_0x22[5:4]/ 0x26[5:4]=10 (default)		12.5		
		Setting by reg_0x22[5:4]/ 0x26[5:4]=11		20		
$t_{OVPDLY\_SWA/B}$	OVP Propagation Delay			5		μs
	UVP Threshold	Setting by reg_0x22[3:2]/ 0x26[3:2]=00 (default)		−10		%
		Setting by reg_0x22[3:2]/ 0x26[3:2]=01		−12.5		

Electrical Characteristics(Continued)

Limits apply over the full operating ambient temperature range (0°C ≤ T_A ≤ +85°C) and V_{INA} = V_{INB} = V_{INC} = V_{IN} = 5V, typical values are at T_A=+25°C, unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
	UVP Threshold	Setting by reg_0x22[3:2]/ 0x26[3:2]=10		−7.5		%
		Setting by reg_0x22[3:2]/ 0x26[3:2]=11		−20		
$t_{UVPDLY\_SWA/B}$	UVP Propagation Delay			5		µs
$I_{LIM\_SWA/B}$	Current Limit	Valley current limited Setting by reg_0x20[7:6]/[3:2]=00(default)		5.0		A
		Setting by reg_0x20[7:6]/[3:2]=01		5.5		
		Setting by reg_0x20[7:6]/[3:2]=10		6.0		
SWC						
V_{OUT_SWC}	Output Voltage Setting		1.5	1.8	2.135	V
V_{OUT_SWC}	Output Voltage Accuracy	I_{out} = 0, CCM	−0.75		0.75	%
	Dynamic Voltage Scale slew rate			1		mV/µs
	Soft-start Time	t_{set} = 1ms to 14ms	−15		15	%
	Soft-stop Time	t_{set} = 0.5ms to 4ms	−20		20	%
$R_{DS(ON)\_SWC}$	High side MOSFET $R_{DS(ON)}$			50		mΩ
$R_{DS(ON)\_SWC}$	Low side MOSFET $R_{DS(ON)}$			40		mΩ
f_{SW_SWC}	Switching Frequency	Setting by reg_0x2A[1:0]=00 (default)	−15%	0.75	+15%	MHz
		Setting by reg_0x2A[1:0]=01	−15%	1.0	+15%	
		Setting by reg_0x2A[1:0]=10	−15%	1.25	+15%	
		Setting by reg_0x2A[1:0]=11	−15%	1.5	+15%	
	OVP Threshold	Setting by reg_0x28[5:4]=00		7.5		%
		Setting by reg_0x28[5:4]=01		10		
		Setting by reg_0x28[5:4]=10 (default)		12.5		
		Setting by reg_0x28[5:4]=11		20		
t_{OVPDLY_SWC}	OVP Propagation Delay			5		µs
	UVP Threshold	Setting by reg_0x28[3:2]=00 (default)		−10		%
		Setting by reg_0x28[3:2]=01		−12.5		
		Setting by reg_0x28[3:2]=10		−7.5		
		Setting by reg_0x28[3:2]=11		−20		
t_{UVPDLY_SWC}	UVP Propagation Delay			5		µs

Electrical Characteristics(Continued)

Limits apply over the full operating ambient temperature range (0°C ≤ T_A ≤ +85°C) and V_{INA} = V_{INB} = V_{INC} = V_{IN} = 5V, typical values are at T_A=+25°C, unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$I_{LIM\_SWC\_LOWCurrent}$	Current Limit	Valley current limited Setting by reg_0x20[1:0]=00		0.5		A
		Setting by reg_0x20[1:0]=01		1.0		
		Setting by reg_0x20[1:0]=10		1.5		
		Setting by reg_0x20[1:0]=11(default)		2		
VLDO_1.8V (1.8V, IMAX = 25mA)						
$V_{LDO\_1.8V}$	Output Voltage	Setting by reg_0x2B[7:6]=00	−2.0%	1.7	+2.0%	V
		setting by reg_0x2B[7:6]=01 (default)	−2.0%	1.8	+2.0%	
		Setting by reg_0x2B[7:6]=10	−2.0%	1.9	+2.0%	
		Setting by reg_0x2B[7:6]=11	−2.0%	2.0	+2.0%	
	Current Limit			200		mA
VLDO_1.0V (1.0V, IMAX = 20mA)						
$V_{LDO\_1.0V}$	Output Voltage	Setting by reg_0x2B[2:1]=00	−2.0%	0.9	+2.0%	V
		setting by reg_0x2B[2:1]=01 (default)	−2.0%	1.0	+2.0%	
		Setting by reg_0x2B[2:1]=10	−2.0%	1.1	+2.0%	
		Setting by reg_0x2B[2:1]=11	−2.0%	1.2	+2.0%	
	Current Limit			200		mA
Logic Interface DC Electrical Specification						
V_{IL}	Input Low Voltage (PWR_GOOD, SDA, SCL, VR_EN)		−0.3		0.3	V
V_{IH}	Input High Voltage (SDA, SCL)		0.7		3.6	V
	Input High Voltage (PWR_GOOD, VR_EN)		1.26		3.6	
V_{OL}	Output Low Voltage (SDA, PWE_GOOD, GSI_n)				0.3	V
V_{OH}	Output High Voltage (SDA)		0.75			V
I_{OL}	Output Low Current (SDA, PWR_GOOD, GSI_n)				3	mA
I_{OH}	Output High Current (SDA)		−3			mA
I_{LI}	Input Leakage Current				±5	μA
I_{LO}	Output Leakage Current				±5	μA
SR	Rising Output Slew Rate (SDA)		0.1		1	V/ns

Electrical Characteristics(Continued)

Limits apply over the full operating ambient temperature range (0°C ≤ T_A ≤ +85°C) and V_{INA} = V_{INB} = V_{INC} = V_{IN} = 5V, typical values are at T_A=+25°C, unless otherwise specified.)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SR	Falling Output Slew Rate (SDA)		0.1		3	V/ns
f_{SCL,I^2C}	I^2C operate Frequency		0.01		1	MHz
f_{SCL,I^3C}	I^3C operate Frequency		0.01		12.5	MHz

6 Functional Description

6.1 Block Diagram

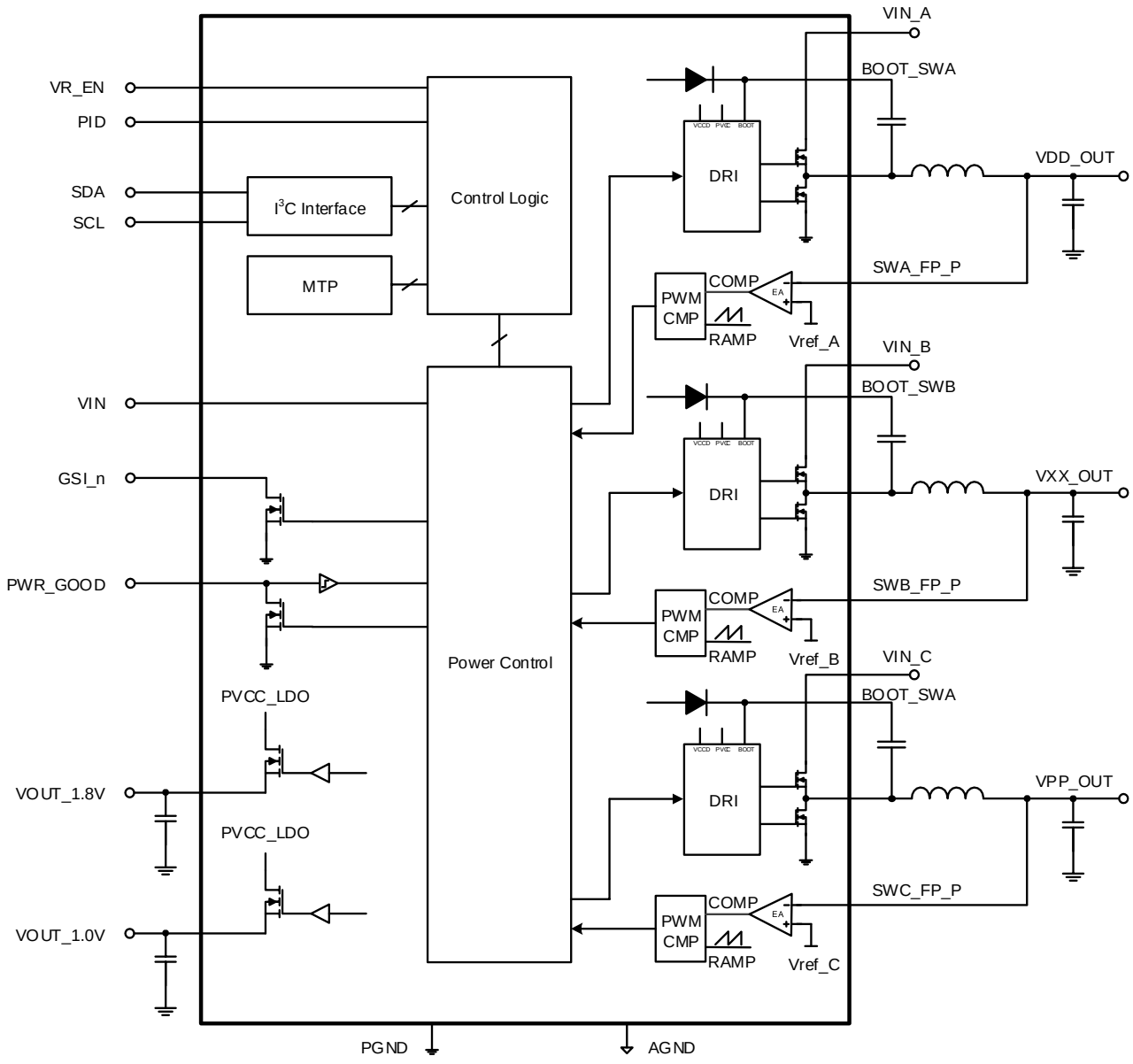


Figure 1. Block Diagram for GD30MP1020

6.2 Operation

6.2.1 PMIC Input Voltage Supply and Ramp Condition

The GD30MP1020 has one input supply from the platform: VIN_Bulk.

The VIN_Bulk supply is used by the PMIC for all three switch (SWA, SWB, SWC) output regulators and two LDO outputs (VOUT_1.8V & VOUT_1.0V) regulators. Note that the VOUT_1.8V LDO output is separate and independent from SWC output, which is for the DRAM VPP rail. The VOUT_1.0V LDO output is separate and independent from SWA or SWB.

At first power on, the VIN_Bulk input supply shall reach a minimum threshold voltage of 4.25V before it can be detected as a valid input supply to the PMIC.

Once the VIN_Bulk supply is valid and stable, the PMIC shall assert PWR_GOOD output low, drive VOUT_1.8V & VOUT_1.0V supply within $t_{1.8V\_Ready}$ and $t_{1.0V\_Ready}$ time respectively. The PMIC drives PWR_GOOD output signal low only when VIN_Bulk input supply reaches minimum of 4.25V. The PWR_GOOD output is pulled up to either 1.8V or 3.3V on the platform or on the host controller.

The PWR_GOOD pull up voltage (either 1.8V or 3.3V) can be available before or after VIN_Bulk is valid and stable. If PWR_GOOD pull up voltage is available before VIN_Bulk is applied, the PWR_GOOD signal is High and remains High with no leakage path or damage to the PMIC. When VIN_Bulk is applied to the PMIC, the PMIC asserts PWR_GOOD output low.

The PMIC shall enable I^2C/I^3C bus interface function within $t_{Management\_Ready}$. The host shall not attempt to access the PMIC's memory registers until $t_{Management\_Ready}$ timing requirement is satisfied.

6.2.2 Power Up Initialization Sequence

During power on, the host shall:

[1] Ramp up VIN_Bulk supply.

[2] Hold VIN_Bulk supply stable for a minimum of $t_{VIN\_Bulk\_to\_VR\_Enable}$ time.

[3] Hold VR_EN pin to static low or high.

[4] During VIN_Bulk ramp, if VR_EN signal is held low, it can transition to high only once. Once high, it shall remain high. The VR_EN signal is not allowed to transition to low during VIN_Bulk ramp up.

[5] If VR_EN pin is held High during VIN_Bulk ramp up or transitions to High during VIN_Bulk ramp up, the PMIC turns on its output rails.

[6] If VR_EN pin is held Low during VIN_Bulk Ramp, assert VR_EN signal High to turn on PMIC output rails. Alternatively, host can issue VR Enable command by setting register 0x32[7] = 1 via I^2C/I^3C Basic bus or via DEVCTRL CCC to turn on PMIC output rails.

Figure 2 to Figure 6 shows example of PMIC power up initialization sequence. Note that the specific sequence of ramping the output regulators (SWA, SWB, SWC) is for example purpose only. The specific ramp up sequence is configurable through power on sequence configuration registers.

After VR Enable command is registered on the I^2C or I^3C Basic bus or VR_EN pin is registered high, the PMIC

shall complete the following steps within $t_{PMIC\_PWR\_GOOD\_OUT}$:

[1] Check VIN_Bulk Power Good status is valid.

[2] Power up itself – GD30MP1020 executes Power On Sequence Config0 to Power On Sequence Config2 registers and configures GD30MP1020 internal registers as programmed in DIMM vendor memory space registers.

[3] Power up all enabled output switch regulators and ready for normal operation.

[4] Update status registers 0x08[5,3:2] and floats PWR_GOOD signal within maximum of $t_{PMIC\_PWR\_GOOD\_OUT}$ time.

[5] If PMIC PWR_GOOD signal is not floated within $t_{PMIC\_PWR\_GOOD\_OUT}$ time, the host can access the PMIC status registers for detailed information after $t_{PMIC\_PWR\_GOOD\_OUT}$ time. The PMIC may NACK for any host request on I^2C or I^3C Basic bus after VR Enable command (either with VR_EN pin high or on I^2C/I^3C Basic Bus) until $t_{PMIC\_PWR\_GOOD\_OUT}$ time expires.

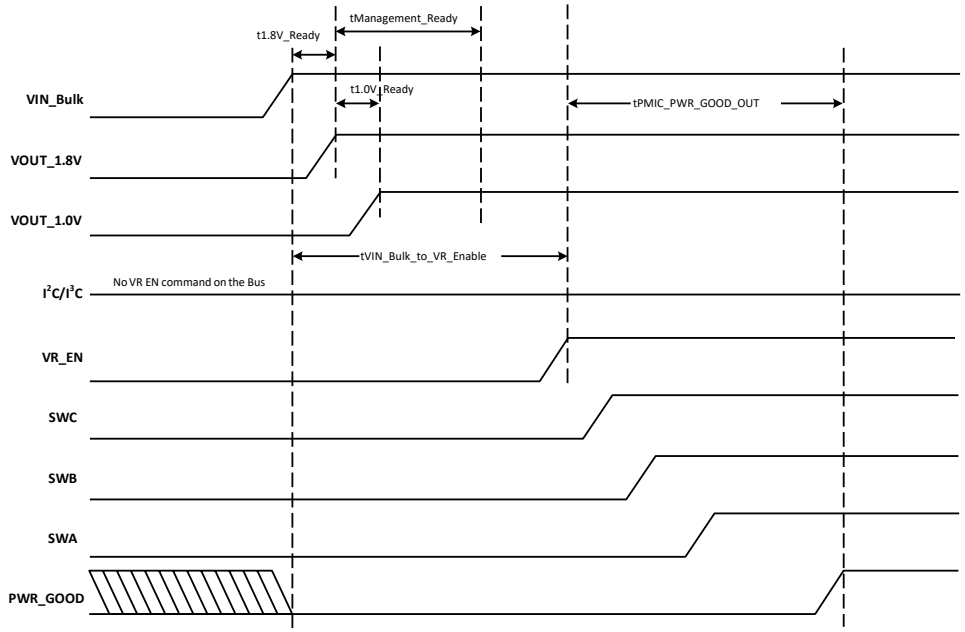


Figure 2. Power Up Sequence; VR_EN pin High after VIN_Bulk Ramp; No Bus Command

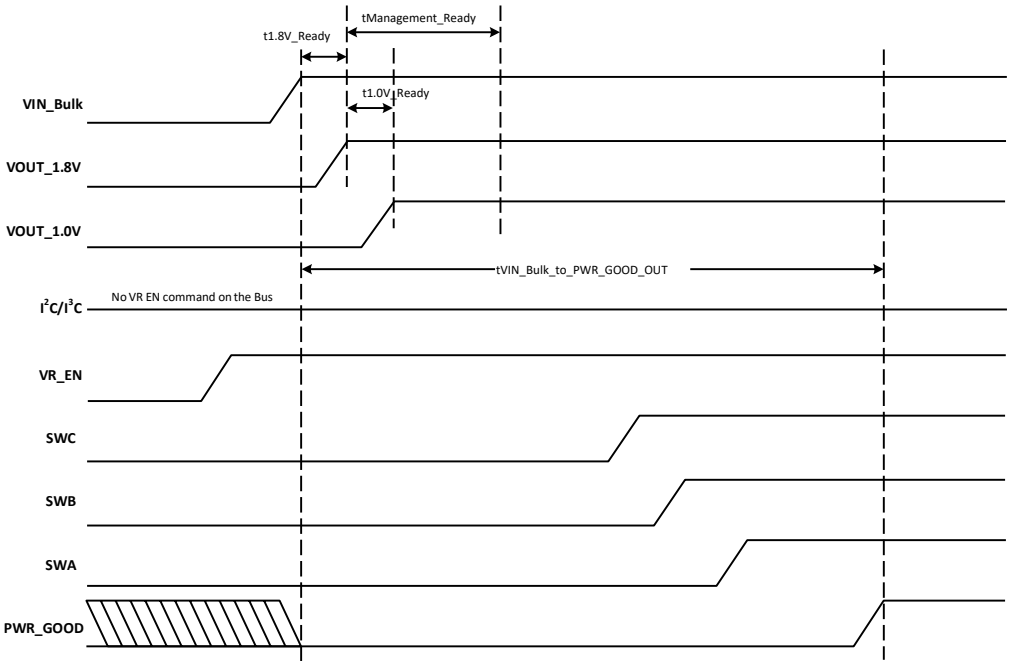


Figure 3. Power Up Sequence; VR_EN pin High before VIN_Bulk Ramp; No Bus Command

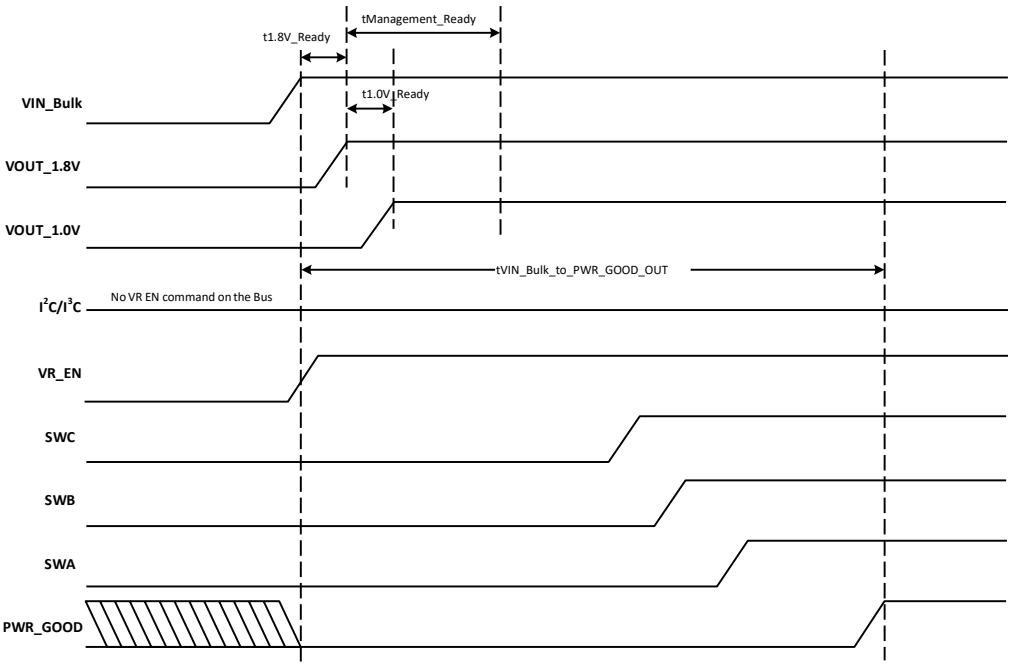


Figure 4. Power Up Sequence; VR_EN pin High during VIN_Bulk Ramp; No Bus Command

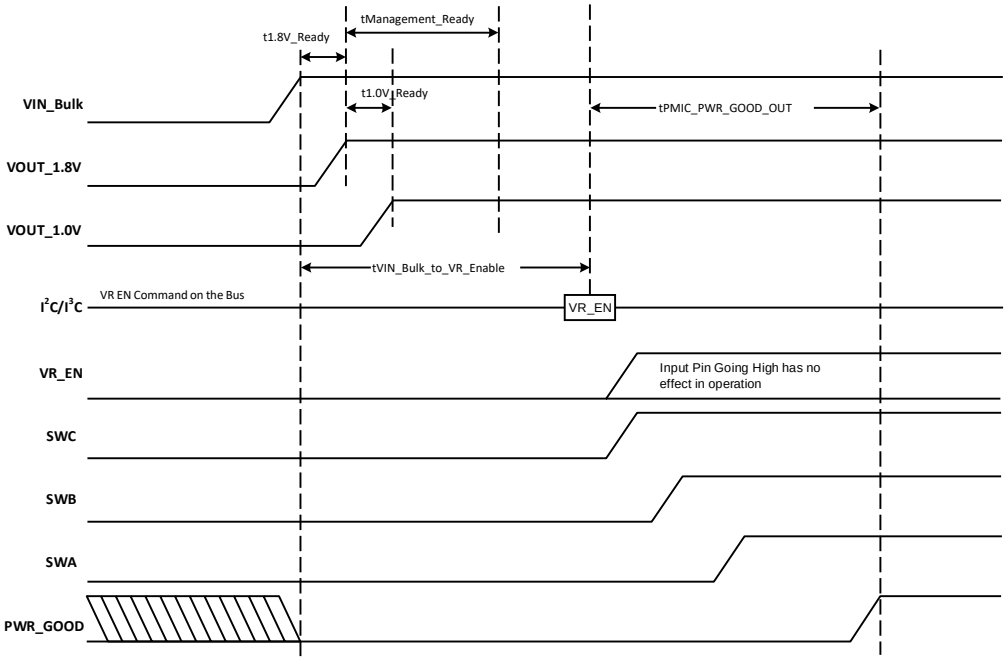


Figure 5. Power Up Sequence; With VR_EN Bus Command

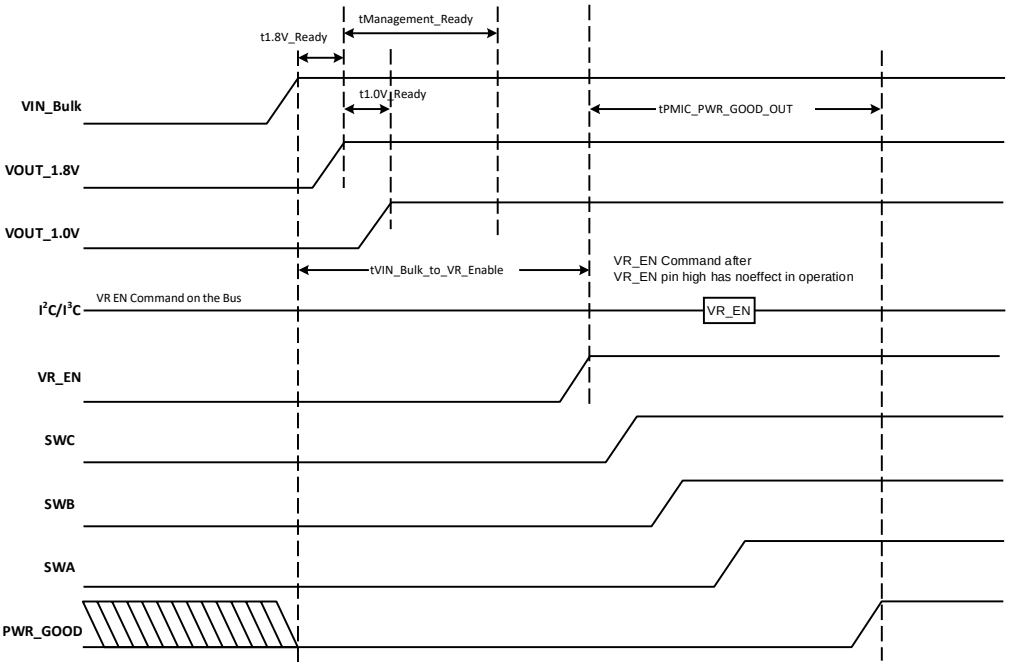


Figure 6. Power Up Sequence; With VR_EN Pin

6.2.3 Turn On Timing of PMIC Output Rail

The Figure 7 below shows the timing relationship once the PMIC receives VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus) and when it floats PWR_GOOD output signal; timing parameter $t_{PMIC\_PWR\_GOOD\_OUT}$ applies. This timing parameter is a sum of maximum soft start time and configured delay for each power on sequence configuration registers that are executed plus additional 5 ms timing margin error. The waveform shows each buck regulator output soft start time and delay time once the soft start time expires for each power on sequence config0 to power on sequence config2 registers. Note that if more than one regulators are enabled in a power on sequence config register and if those regulators have different soft start time programmed, then the larger value of that soft start time is used as a reference for delay timer to start. Each regulator will still follow different soft start time to turn on the buck regulator.

The specific example in Figure 7 uses three power on sequence config0 to config2 registers and only one buck regulator is enabled in each power on sequence config0 to config2 registers.

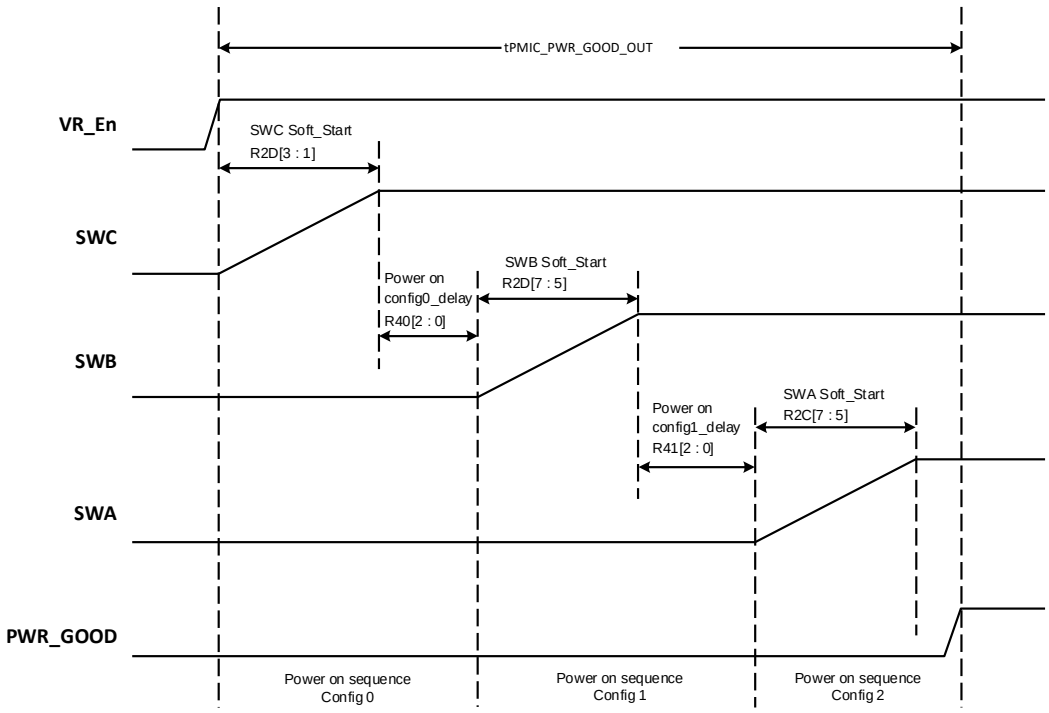


Figure 7. GD30MP1020 Power On Timing

6.2.4 Secure Mode & Programmable Mode of Operation

Prior to issuing VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus), the host must configure the register “Register 0x2F” [2] appropriately as desired. The PMIC offers two modes of operation after VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus) is registered.

[1] Programmable Mode-In this mode, independent of when host issues VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus), the PMIC allows modification to any register in the host region as desired by the host and PMIC responds appropriately.

[2] Secure Mode-In this mode, after host issues VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus), the PMIC does not allow modification to registers, “Register 0x15” to “Register 0x2F”, “Register0x32”

[7,5:0] in the host region as well as “Register 0x40” to Register 0x6F in the DIMM vendor region. These registers are writen protected. The host must power cycle the PMIC to make any modification. The PMIC power cycle is defined as complete removal of VIN_Bulk input supply to the PMIC and this definition is applied to the entire specification. The Secure Mode is only applicable once VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus) is registered. This is important because by default, “Register 0x2F” [2] =‘0’when PMIC is first powered up. Prior to VR Enable command (either with VR_EN pin or on I²C/I³C Basic bus), PMIC allows modification to any registers in the host region.

6.2.5 Power Down Output Regulators

Regardless of how PMIC’s output regulators are turned on (w/VR_EN pin or w/VR Enable command on I²C/I³C Basic bus), the PMIC’s output regulators are powered down as described below depending on PMIC’s mode of operation.

Programmable Mode Operation; R1A [4] = 0

The PMIC allows host to power down any or all output regulators by any of the three methods below.

[1] The VR Disable command (Register 0x32[7] = 0 or VR_EN pin transitions to low). The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers. The PMIC controls the PWR_GOOD signal as following in (a) and (b):

(a) If VR Disable command with a pin (i.e. VR_EN pin transitions to Low), PMIC asserts PWR_GOOD signal Low. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High. The PMIC executes power on sequence config0 to config2 registers and floats PWR_GOOD signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied.

(b) If VR Disable command on a I²C/I³C Bus (i.e. Register 0x32[7] = 0), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The host can re-enable the PMIC’s output regulators by issuing VR_EN command on the I²C/I³C bus (i.e. Register 0x32[7] = 1). The PMIC executes power on sequence config0 to config2 registers and continues to float the PWR_GOOD signal until $t_{PMIC\_PWR\_GOOD\_OUT}$ time at which point, PMIC assumes normal control of PWR_GOOD signal.

(c) The simultaneous usage of VR_EN pin and I²C/I³C bus command to turn on/off the PMIC is not allowed. If the VR_EN pin transitions to Low first, the PWR_GOOD signal follows as described in (a) and PWR_GOOD signal remains low even if there is a subsequent I²C/I³C bus command as described in (b).

[2] Configuring one or more bits in register 0x2F [6,4:3] to ‘0’ in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 to config2 on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in register 0x2F[6,4:3] to ‘1’ in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating.

[3] If register 0x32[5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. If host re-enables PMIC’s output regulators by issuing VR_EN command on the I2C/I3C Basic bus (i.e. register

0x32[7] = 1), the PMIC executes power on sequence config0 to config2 registers and floats PWR_GOOD output signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in “Trigger VR Disable”.

The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers. The PMIC asserts PWR_GOOD signal low. The host can re-enable PMIC’s output regulators with VR Enable command with either register 0x32[7] = 1 or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

Programmable Mode Operation; R1A [4] = 1

The PMIC allows host to power down any or all output regulators by any of the three methods below.

[1] The VR Disable command (Register 0x32[7] = 0 or VR_EN pin transitions to low). The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The PMIC controls the PWR_GOOD signal as following in (a) and (b):

(a) If VR Disable command with a pin (i.e. VR_EN pin transitions to Low), PMIC asserts PWR_GOOD signal Low. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and executes power on sequence config0 to config 2 registers and floats PWR_GOOD signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied.

(b) If VR Disable command on a I^2C/I^3C Basic Bus (i.e. Register 0x32[7] = 0), PMIC keeps the PWR_GOOD signal floating because this is an intentional command from the host and not a fault condition. The PMIC exits from P1 state with only VR_EN pin transition to High. The host can re-enable the PMIC’s output regulators by VR_EN pin transition to High and PMIC executes power on sequence config0 to config2 registers. The PMIC continues to float PWR_GOOD signal until $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied and at that point PMIC assumes normal control of PWR_GOOD signal.

[2] Configuring one or more bits in register 0x2F [6,4:3] to 0 in any specific sequence that is desired by the host. The PMIC does not execute power off sequence config0 to config2 on its own. The PMIC keeps the PWR_GOOD signal floating because this is intentional command from the host and not a fault condition. Note that host can re-enable any of disabled output regulators by configuring one or more bits in register 0x2F [6,4:3] to 1 in any specific sequence that is desired by the host. The PMIC keeps the PWR_GOOD signal floating.

[3] If register 0x32[5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers and drives PWR_GOOD signal low. The PMIC preserves all register contents including the MTP error log registers. The PMIC does not enter in P1 state. If host re-enables PMIC’s output regulators by issuing VR_EN command on I2C/I3C Basic bus (i.e. Register 0x32[7] = 1), the PMIC executes power on sequence config0 to config2 registers and floats PWR_GOOD signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied. The PMIC does not require power cycle.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in “Trigger VR Disable”. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The host can re-enable PMIC’s output regulators with VR Enable command with either

register 0x32[7] = 1 or VR_EN pin transitions to high and PMIC turns on its output regulators and floats PWR_GOOD signal. The PMIC does not require power cycle.

Secure Mode Operation; R1A [4] = 0

The PMIC allows host to power down any or all output regulators by any of the two methods below.

[1] The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC executes power on sequence config0 to config2 registers and floats PWR_GOOD signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied. Note that VR Disable or Enable command on I^2C/I^3C Basic Bus (i.e. Register 0x32[7] = 0 or 1) has no effect on the PMIC. Also, configuring one or more bits in register 0x2F [6,4:3] to 0 has no effect on the PMIC.

[2] If register 0x32[5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only register 0x32 [7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the register 0x32[7]. When host issues VR Enable command by I^2C/I^3C Basic bus, the PMIC executes power on sequence config0 to config2 registers, floats PWR_GOOD output signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied and re-locks register 0x32[7]. The PMIC does not require power cycle to re-enable PMIC's output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in "Trigger VR Disable". The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either register 0x32[7] = 1 or VR_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

Secure Mode Operation; R1A [4] = 1

The PMIC allows host to power down any or all output regulators by any of the two methods below.

[1] The VR Disable command with VR_EN pin transitions to low. The PMIC asserts PWR_GOOD signal Low. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers and enters in P1 state. The host can re-enable the PMIC's output regulators by VR_EN pin transition to High. The PMIC exits from P1 state and execute power on sequence config0 to config2 registers and floats PWR_GOOD signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied. Note that VR Disable or Enable command on a I^2C/I^3C Basic Bus (i.e. Register 0x32[7] = 0 or 1) has no effect on the PMIC. Also, configuring one or more bits in register 0x2F [6,4:3] to 0 has no effect on the PMIC.

[2] If register 0x32[5] = 1, driving PWR_GOOD input low. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers; drives PWR_GOOD signal low and unlocks only register 0x32[7]. The PMIC preserves all register contents including the MTP error log registers and keeps all write protect registers locked except for the register 0x32[7]. The PMIC does not enter in P1 state. When host issues VR Enable command by I^2C/I^3C Basic bus, the PMIC executes Power on sequence config0 to config2 registers, floats PWR_GOOD output signal after $t_{PMIC\_PWR\_GOOD\_OUT}$ timing parameter is satisfied and re-locks register 0x32[7]. The PMIC does not require power cycle to re-enable PMIC's output regulators.

The PMIC, on its own, can generate internal VR Disable command at any time due to one or more events listed in “Trigger VR Disable”. The PMIC executes power off sequence config0 to config2 to preserve the appropriate voltage relationship as configured in the registers. The PMIC does not enter in P1 state. The PMIC assert PWR_GOOD signal low. The PMIC requires power cycle. The VR Enable command with either register 0x32[7] = 1 or VR_EN pin transitions to high has no effect on PMIC and PMIC keeps it PWR_GOOD signal low.

Turn Off Timing of PMIC Output Rail

The Figure 8 below shows the timing relationship once the PMIC registers VR Disable command internally due to fault condition as listed in “Events Interrupt Summary”. The waveform shows each buck regulator output soft stop time and delay time once the soft stop time expires from each power off sequence config0 to config2 registers. Note that if more than one regulators are disabled in a power off sequence config register and if those regulators have different soft stop time programmed, then the larger value of that soft stop time is used as a reference for delay timer to start. Each regulator will still follow different soft stop time to turn off the buck regulator.

The specific example in Figure 8 uses only three power off sequence config0 to config2 registers and only one buck regulator is disabled in power off sequence config0, config1 and config2 registers.

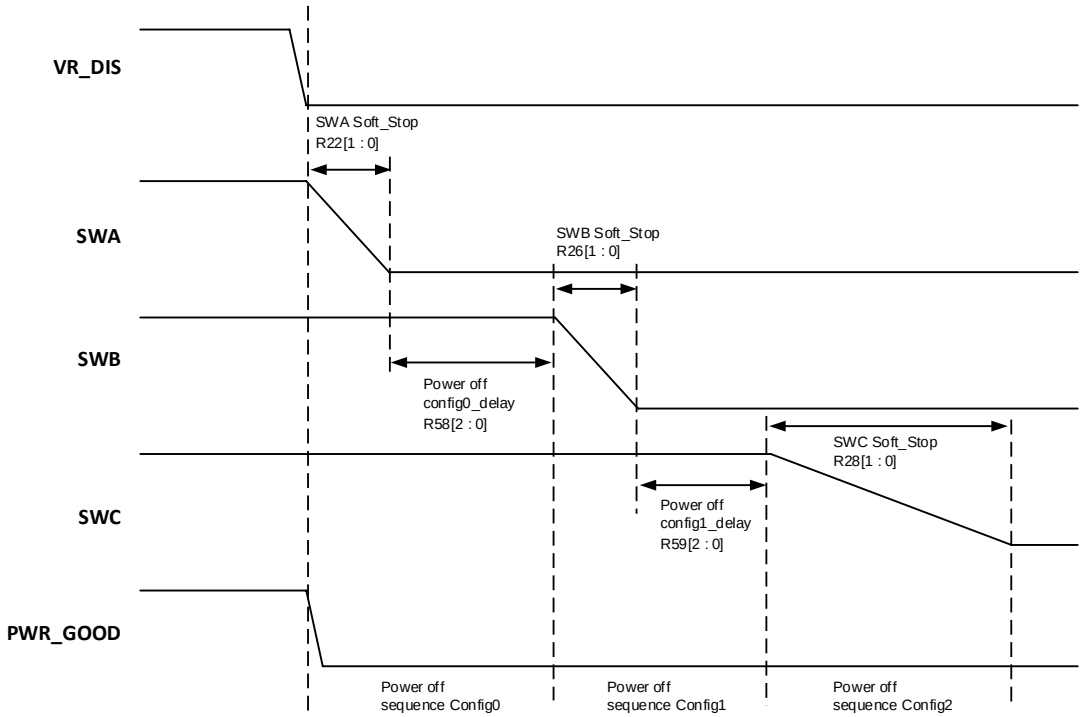


Figure 8. PMIC Power Off Timing Due to Internal Fault Condition

6.2.6 Idle State and Quiescent Power State

Quiescent Power State definition: VIN_Bulk nominal = 5.0V. All circuits including PMIC switch output and LDO output regulators are off. VR_EN signal is at static low or high level. I^2C or I^3C Basic interface access is not allowed and is pulled high. PID signal is at static low or high level. This state is only applicable if register 0x1A [4] = 1. This state is labeled as P1 state in Table 1 below.

Idle Power State definition: VIN_Bulk nominal = 5.0V. All circuits including PMIC switch output and LDO output regulators are on with 0A load. VR_EN signal is at static low or high level. I^2C or I^3C Basic interface access is allowed but bus is pulled high. PID signal is at static low or high level. This state is only applicable if register 0x1A [4] = 0. This state is a same state as P3 state but load on all switch outputs regulators and LDO output regulators is 0A.

Table 1. High Level Finite State Description

State	Description
P0	VIN_Bulk invalid
P1	R1A[4] = '1' Entry from P3 State Only
P2_A1 (No Fault Event)	Transition from P3; After VR Enable Command All Switch Regulators are Off All LDOs are ON PWR_GOOD Output = L or H VR_EN Input = L or H R32[7] = '0'
P2_A2 (Fault Event)	Transition from P3; After VR Enable Command All Switch Regulators are Off All LDOs are ON PWR_GOOD Output = L VR_EN Input = L or H R32[7] = '0'
P2_B	Transient from P0 or P1 State; Before VR Enable Command All Switch Regulators are Off All LDOs are on PWR_GOOD Output = L VR_EN Input = L R32[7]='0'
P3 (Regulation Mode or Bulk Link Monitor Mode)	All Switch Regulators are On R32[7] = '1'

6.2.7 GSI_n Signal

General Status Interrupt (GSI_n) is an Open Drain output signal. By default at power on, GSI_n output is disabled. The host can enable the GSI_n output by setting register 0x1B[3] = 1. Typically, GSI_n output is pulled up to 10KΩ resistor to 1.8 V or 3.3 V. The PMIC asserts GSI_n output for the events as described in Table 2.

6.2.8 Function Interrupt - PWR_GOOD and GSI_n Output Signals

This section defined the output functionality of GSI_n pin and PWR_GOOD pin.

When mask register bits are not set, the PMIC asserts its GSI_n output and assert PWR_GOOD output signals as shown in Table 2 when any event occurs. The table also highlights the events that cause PMIC to generate internally VR Disable command. For remaining events that does not trigger internal VR Disable command, the PMIC continues to operate as normal.

Table 2. Events Interrupt Summary

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	PWR_GOOD Output	GSI_n
VIN_Bulk Over Voltage	R08[0]	R10[0]	R15[0]	R1B[7]	Yes	Low	Low
SWA Output Power Good	R08[5]	R10[5]	R15[5]	R22[5:4] R22[3:2]	No	Low	Low
SWB Output Power Good	R08[3]	R10[3]	R15[3]	R26[5:4] R26[3:2]	No	Low	Low
SWC Output Power Good	R08[2]	R10[2]	R15[2]	R28[5:4] R28[3:2]	No	Low	Low
1.8V LDO Power Good	R09[5]	R11[5]	R16[5]	R1A[2]	No	Low	Low
1.0V LDO Power Good	R33[2]	R14[2]	R19[2]	R1A[0]	No	Low	Low
SWA Output Over Voltage	R0A[7]	R12[7]	R17[7]	R22[5:4]	Yes	Low	Low
SWB Output Over Voltage	R0A[5]	R12[5]	R17[5]	R26[5:4]	Yes	Low	Low
SWC Output Over Voltage	R0A[4]	R12[4]	R17[4]	R28[5:4]	Yes	Low	Low
SWA Output Under Voltage	R0B[3]	R13[3]	R18[3]	R22[3:2]	Yes	Low	Low
SWB Output Under Voltage	R0B[1]	R13[1]	R18[1]	R26[3:2]	Yes	Low	Low
SWC Output Under Voltage	R0B[0]	R13[0]	R18[0]	R28[3:2]	Yes	Low	Low
SWA Output Current Limit	R0B[7]	R13[7]	R18[7]	R20[7:6]	No	High	Low
SWB Output Current Limit	R0B[5]	R13[5]	R18[5]	R20[3:2]	No	High	Low
SWC Output Current Limit	R0B[4]	R13[4]	R18[4]	R20[1:0]	No	High	Low
SWA Output High Current /Power	R09[3]	R11[3]	R16[3]	R20[7:6]	No	High	Low
SWB Output High Current /Power	R09[1]	R11[1]	R16[1]	R20[3:2]	No	High	Low

Status Event	Status Bit	Clear Bit	Mask Bit	Threshold Setting	VR Disable Trigger?	PWR_GOOD Output	GSI_n
SWC Output High Current /Power	R09[0]	R11[0]	R16[0]	R20[1:0]	No	High	Low
High Temperature Warning	R09[7]	R11[7]	R16[7]	R1B[2:0]	No	High	Low
Critical Temperature	R08[6]	N/A	N/A	R2E[2:0]	Yes	Low	Low
PEC Error	R0A[3]	R12[3]	R17[3]	N/A	No	High	Low
Parity Error	R0A[2]	R12[2]	R17[2]	N/A	No	High	Low

The host is expected to read appropriate status registers to determine and isolate the cause of the GSI_n signal assertion or PWR_GOOD signal assertion. The host may attempt to clear or mask the appropriate corresponding interrupt event. The PMIC keeps the GSI_n signal asserted or PWR_GOOD signal asserted until the appropriate corresponding registers are explicitly cleared or masked by the host. Table 3 and Table 4 shows the PMIC's response of GSI_n signal and PWR_GOOD output signal for each event before and after host issues the Clear command. The Table 3 and Table 4 assumes that all mask bits are either '0' or '1' for simplicity.

Table 3. GD30MP1020 Response for Clear Command by Host 1

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			R2F[1:0] = "00" or "01" or "10"		R2F[1:0] = "00"		R2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_Bulk Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	Low	Low	High	High	Low	High	High	High
SWB Output Power Good	Low	Low	High	High	Low	High	High	High
SWC Output Power Good	Low	Low	High	High	Low	High	High	High
1.8V LDO Power Good	Low	Low	High	High	Low	High	High	High
1.0V LDO Power Good	Low	Low	High	High	Low	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High

Event	Event Occurred; All Mask Bits = "0"		Clear Command; Event Not Present; All Mask Bits = "0"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
			R2F[1:0] = "00" or "01" or "10"		R2F[1:0] = "00"		R2F[1:0] = "00"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current /Power	High	Low	High	High	High	High	High	High
SWB Output High Current /Power	High	Low	High	High	High	High	High	High
SWC Output High Current /Power	High	Low	High	High	High	High	High	High
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Table 4. GD30MP1020 Response for Clear Command by Host 2

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	R2F[1:0] = "01"		R2F[1:0] = "01"		R2F[1:0] = "10"		R2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
VIN_BULK Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Power Good	High	Low	High	High	High	High	High	High
SWB Output Power Good	High	Low	High	High	High	High	High	High
SWC Output Power Good	High	Low	High	High	High	High	High	High
1.8V LDO Power Good	High	Low	High	High	High	High	High	High
1.0V LDO Power Good	High	Low	High	High	High	High	High	High
SWA Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Over Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWB Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWC Output Under Voltage	Low	Low	Low	High	Low	High	Low	High
SWA Output Current Limit	High	Low	High	High	High	High	High	High
SWB Output Current Limit	High	Low	High	High	High	High	High	High
SWC Output Current Limit	High	Low	High	High	High	High	High	High
SWA Output High Current/Power	High	Low	High	High	High	High	High	High
SWB Output High Current/Power	High	Low	High	High	High	High	High	High
SWC Output High Current/Power	High	Low	High	High	High	High	High	High

Event	Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"		Event Occurred; All Mask Bits = "1"		Clear Command; Event Not Present; All Mask Bits = "1"	
	R2F[1:0] = "01"		R2F[1:0] = "01"		R2F[1:0] = "10"		R2F[1:0] = "10"	
	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output	PWR_GOOD Output	GSI_n Output
High Temperature Warning	High	Low	High	High	High	High	High	High
Critical Temperature	Low	Low	Power Cycle	Power Cycle	Low	Low	Power Cycle	Power Cycle
PEC Error	High	Low	High	High	High	High	High	High
Parity Error	High	Low	High	High	High	High	High	High

Note that when host masks any of the event in appropriate register, it only masks the assertion of GSI_n output signal or assertion of PWR_GOOD output signal. The PMIC functional behavior remains the same as noted for each event other than assertion of GSI_n output signal and assertion of PWR_GOOD output signal.

The PMIC assumes that there is no fuse protection on VIN_Bulk input rail on the DDR5 DIMM module to prevent short circuit type event.

6.2.9 Analog-to-Digital Converter (ADC)

The GD30MP1020 supports analog to digital converter (ADC) to monitor input supply voltages (VIN_Bulk) as well as output voltage regulator voltage (SWA, SWB, SWC, VOUT_1.8V and VOUT_1.0V). The register 0x30[7:3] allows to enable the ADC and select the input supply voltage or desired output supply voltage. The register 0x31[7:0] provides the actual voltage measurement. The accuracy of the voltage measurement is as following:

Table 5. ADC Accuracy Table

Input Rail	ADC Range	ADC Accuracy
SWA, SWB Output Voltage	1050mV to 1160mV	±1 LSB
	Outside of 1050mV to 1160mV	±3 LSB
SWC Output Voltage	1750mV to 1850mV	±1 LSB
	Outside of 1750 mV to 1850mV	±3 LSB
VOUT_1.8V, VOUT_1.0V Output Voltage, VIN Input Voltage		±3 LSB

The GD30MP1020 also monitors output voltage regulator current or power (SWA, SWB and SWC) and updates register 0x0C[7:0] for SWA, register 0x0E[5:0] for SWB and register 0x0F[5:0] for SWC. The register 0x1B[6] allows host to select whether GD30MP1020 should report current measurements or power measurements. The current or power measurement reported in these registers are an average measurement over time period defined in register 0x30[1:0]. If register 0x1B[6] = 1, the register 0x1A[1] allows host to select whether GD30MP1020 should report individual rail power or total power in register 0x0C[7:0]. The register updates frequency of this register is configured in register 0x30[1:0]. The accuracy of the current (0.5A to 5A) or corresponding power measurement is ± 3 LSB or ± 6 LSB respectively. The accuracy of the current measurement (< 0.5 A) is ± 4 LSB or corresponding power measurement is ± 7 LSB respectively.

If register 0x1A[1] = 1, the accuracy of total power reported in register 0x0C = ± 12 LSB.

6.2.10 PMIC Address ID (PID)

The GD30MP1020 has PID input pin which allows assigning up to three different unique ID for I^2C and I^3C Basic protocol. At first power on, when VIN_Bulk input is applied, the PMIC automatically determines its ID. The GD30MP1020 offers three different ID as shown in Table 6.

Table 6. PMIC ID

PID Pin Connection on DIMM Board	PMIC ID	Comment
Short to GND	PID = 1001	PMIC can be configured
Floating	PID = 1000	
Short to 1.8V	PID = 1100	Connected to PMIC's VOUT_1.8V

7 Application Information

7.1 Typical Application Circuit

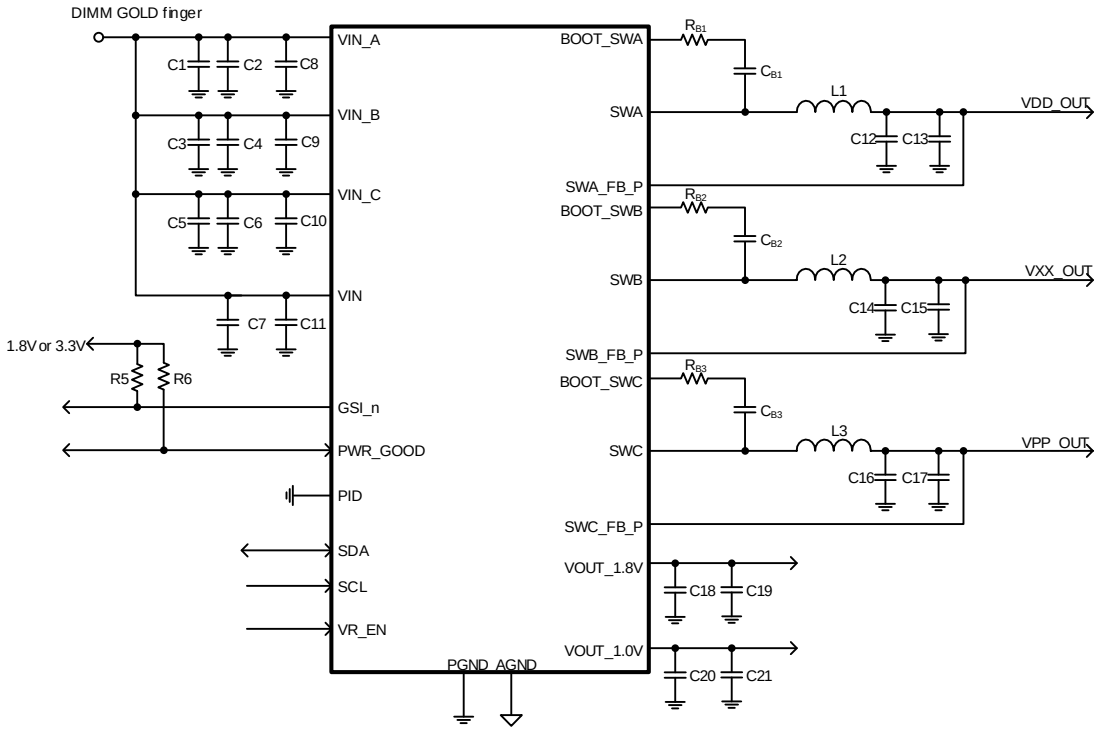


Figure 9. SWA and SWB are operating in Single-Phase Mode

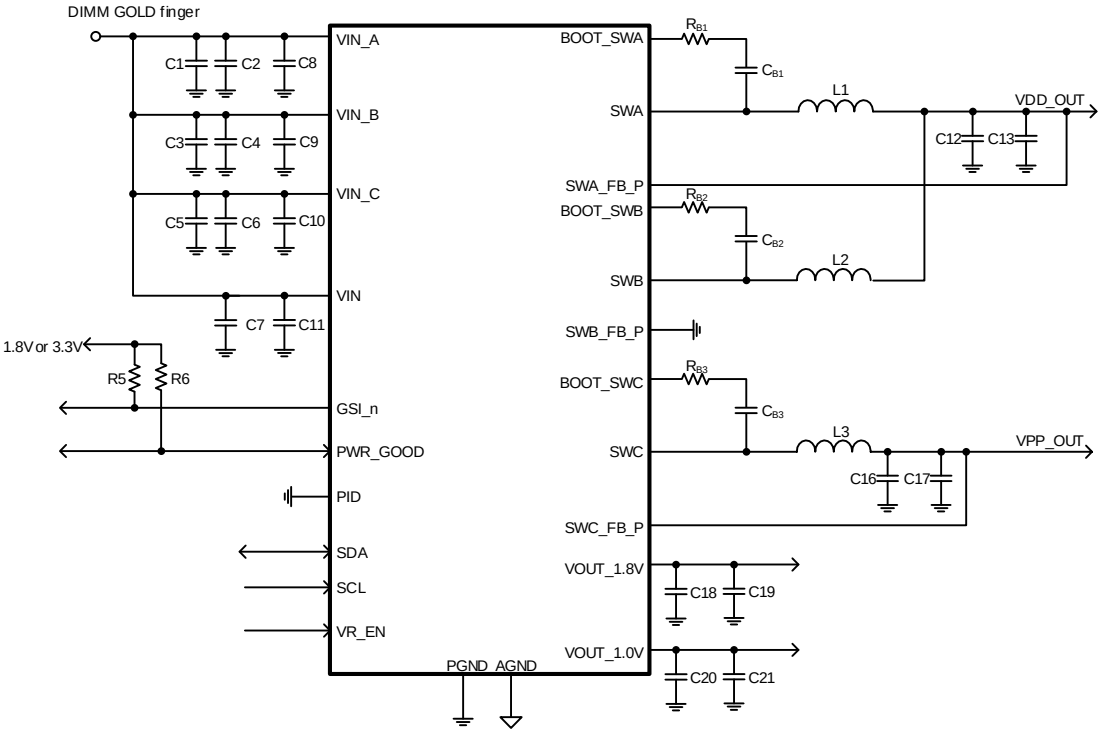


Figure 10. SWA and SWB are operating in Dual-Phase Mode

7.2 Detailed Design Description

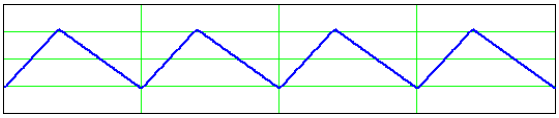
7.2.1 Output Capacitor Selection

The output capacitor is used to keep the DC output voltage and supply the load transient current. When operating in constant current mode, the output ripple is determined by four components:

$$V_{RIPPLE}(t) = V_{RIPPLE(C)}(t) + V_{RIPPLE(ESR)}(t) + V_{RIPPLE(ESL)}(t) + V_{NOISE}(t) \quad (1)$$

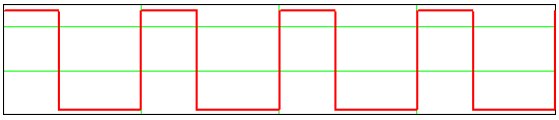
The following figures show the form of the ripple contributions.

$V_{RIPPLE(ESR)}(t)$



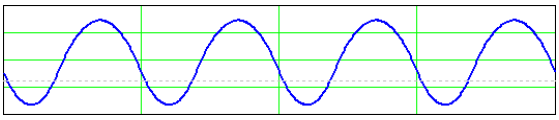
(t)

+ $V_{RIPPLE(ESL)}(t)$



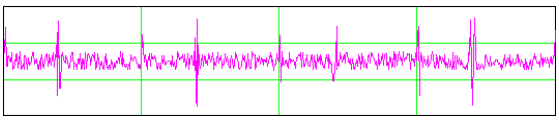
(t)

+ $V_{RIPPLE(C)}(t)$



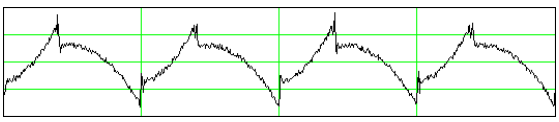
(t)

+ $V_{NOISE}(t)$



(t)

= $V_{RIPPLE}(t)$



(t)

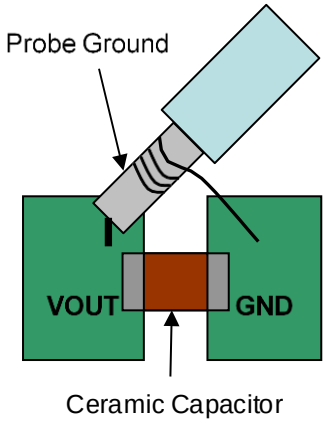
$$V_{RIPPLE(ESR)}=\frac{V_{OUT}}{F_{OSC}\times L}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right)\times ESR \quad (2)$$

$$V_{RIPPLE(ESL)}=\frac{ESL}{L}\times V_{IN} \quad (3)$$

$$V_{RIPPLE(C)}=\frac{V_{OUT}}{8\times F_{OSC^2}\times L\times C_{OUT}}\times\left(1-\frac{V_{OUT}}{V_{IN}}\right) \quad (4)$$

Where F_{OSC} is the switching frequency, L is the inductance value, V_{IN} is the input voltage, ESR is the equivalent series resistance value of the output capacitor, ESL is the equivalent series inductance value of the output capacitor and the C_{OUT} is the output capacitor. Low ESR capacitors are preferred to use. Ceramic, tantalum or low ESR electrolytic capacitors can be used depending on the output ripple requirements. When using the ceramic capacitors, the ESL component is usually negligible.

It is important to use the proper method to eliminate high frequency noise when measuring the output ripple. The figure shows how to locate the probe across the capacitor when measuring output ripple. Remove the scope probe plastic jacket in order to expose the ground at the tip of the probe. It gives a very short connection from the probe ground to the capacitor and eliminates noise.



7.2.2 Input Capacitor Selection

The use of the input capacitor is filtering the input voltage ripple and the MOSFETS switching spike voltage. Because the input current to the step- down converter is discontinuous, the input capacitor is required to supply the current to the converter to keep the DC input voltage. The capacitor voltage rating should be 1.25 to 1.5 times greater than the maximum input voltage. The input capacitor ripple current RMS value is calculated as:

$$I_{IN(RMS)}=I_{OUT}\times\sqrt{D\times(1-D)} \quad (5)$$

$$D=\frac{V_{OUT}}{V_{IN}} \quad (6)$$

Where D is the duty cycle of the power MOSFET.

This function reaches the maximum value at D=0.5 and the equivalent RMS current is equal to $I_{OUT}/2$.

A low ESR capacitor is required to keep the noise minimum. Ceramic capacitors are better, but tantalum or low ESR electrolytic capacitors may also suffice.

7.2.3 Inductor Selection

The output inductor is used for storing energy and filtering output ripple current. But the trade-off condition often happens between maximum energy storage and the physical size of the inductor. The first consideration for selecting the output inductor is to make sure that the inductance is large enough to keep the converter in the continuous current mode.

That will lower ripple current and result in lower output ripple voltage. The ΔI_L is inductor peak-to- peak ripple current:

$$\Delta I_L = \frac{V_{OUT}}{F_{OSC}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

A good compromise value between size and efficiency is to set the peak-to-peak inductor ripple current ΔI_L equal to 30% of the maximum load current. But setting the peak-to-peak inductor ripple current ΔI_L between 20%~50% of the maximum load current is also acceptable. Then the inductance can be calculated with the following equation:

$$\Delta I_L = 0.3 \times I_{OUT(MAX)} \quad (8)$$

$$L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN} \times F_{OSC} \times \Delta I_L} \quad (9)$$

To guarantee the required output current, the inductor needs a saturation current rating and a thermal rating that exceeds I_L (peak current). These are minimum requirements. To maintain control of inductor current in overload and short circuit conditions, some applications may desire current ratings up to the current limit value.

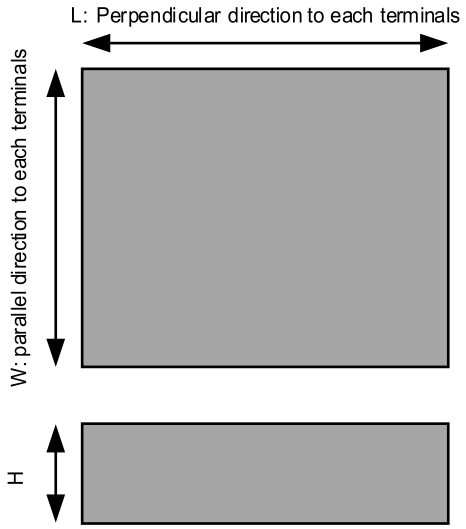
Since DDR5 on DIMM has layout space constraints on the power management IC on the DIMM and surrounding components such as inductors and input/output capacitors, the mechanical specifications for standard inductors are defined in Table 7 and Table 8.

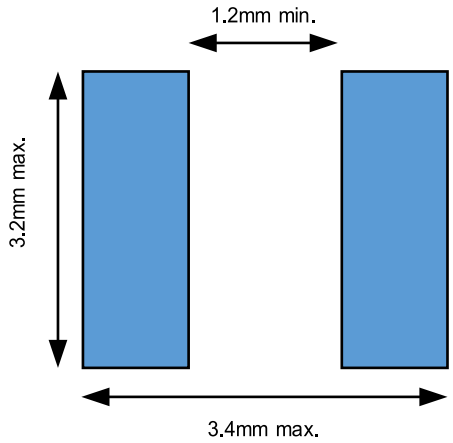
Electrical specifications include inductance, maximum DCR, maximum ACR, and minimum inductance requirements after specified operating current de-rating. DIMM vendors can select inductors according to Table 9.

Since the inductor size is fixed, the trade-off between efficiency and transient response is the main consideration in selection. In general, the inductance of SWA and SWB is recommended to be chosen between 0.47μH and 0.68μH for a 1.1V output rail. The output voltage rail of SWC is 1.8V, and the inductor is recommended to be selected between 1.0μH and 1.5μH.

Table 7. SWA & SWB Inductor Mechanical Specifications

Package Size		
L (mm)	W (mm)	H (mm)
3.4 max.	3.2 max.	1.2 max.

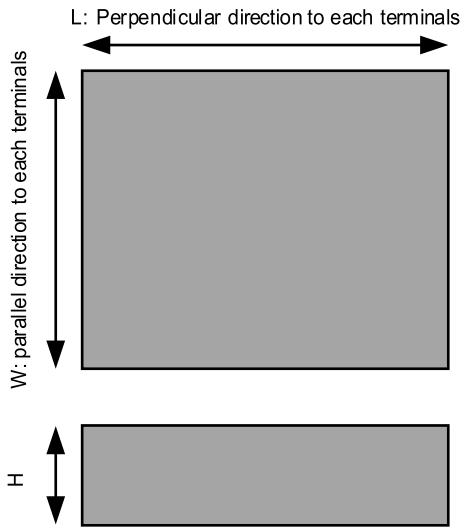


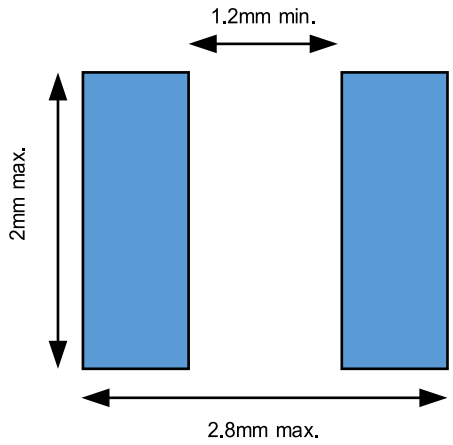


Reference Drawings	Land Pattern

Table 8. SWC Inductor Mechanical Specifications

Package Size		
L (mm)	W (mm)	H (mm)
2.7 max.	2.2 max.	1.2 max.





Reference Drawings	Land Pattern

Table 9. Inductor Electrical Specification

Output inductor	L @ 0.5-1 MHz; 0 Bias (μH)	Max DCR (mΩ)	Max ACR @ 1MHz (mΩ)	Min L @ 6A (μH)
SWA & SWB	0.47 ± 20%	14.5	93	0.30
	0.68 ± 20%	18.5	113	0.38
SWC	1.0 ± 20%	48.0	182	0.56
	1.5 ± 20%	75.0	300	0.82

Table 10. I Input & Output Capacitor Electrical Specification

Component	Value	Physical Size
C_{IN}	4.7μF	10V / 0402
	0.1μF	10V / 0201
C_{INA}	22μF (x2)	10V / 0402
	0.1μF	10V / 0201
C_{INB}	22μF (x2)	10V / 0402
	0.1μF	10V / 0201
C_{INC}	22μF (x2)	10V / 0402
	0.1μF	10V / 0201
C_{B1}、C_{B2}、C_{B3}	0.1μF	10V / 0201
C_{OUTA}	47μF (x2)	6.3V / 0603
C_{OUTB}	47μF (x2)	6.3V / 0603
C_{OUTC}	47μF (x2)	6.3V / 0603
C_{DISTA}	350μF	6.3V
C_{DISTB}	350μF	6.3V
C_{DISTC}	150μF	6.3V
$C_{OUT\_1.8V}$	4.7μF	6.3V / 0402
	0.1μF	6.3V / 0201
$C_{OUT\_1.0V}$	4.7μF	6.3V / 0402
	0.1μF	6.3V / 0201

Note that capacitors C_{DISTA}, C_{DISTB} and C_{DISTC} represent the lump sum of distributed capacitance across the entire DIMM.

8 Register Description

8.1 Register Attribute Definition

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by host. Writes have no effect.
Read / Write	RW	This bit can be read or written by host.
Write Only	WO	This bit can only be written by host. Read from this bit returns”0”.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by host. The bit will return”0” when read. Write has no effect.
Write 1 Only	1O	This bit can only be set (i.e. write”1”) but not reset (i.e. write”0”). Write ”0” has no effect.
Protected	P	This bit is protected by the password. This bit cannot be read or written to unless the password code has been written into the password registers.
Persistent	E	This bit is persistent during power cycle.

8.2 Register Map Breakdown

Register Range	Region	Description
0x15 - 0x2F, 0x32	Host Region	Host accessible registers. Register modification is NOT allowed in Secure Mode.
0x40 - 0x6F	DIMM Vendor Region	Non-Volatile Memory. These registers require password for read access. Access to these registers without correct password will return all data as ‘0’. These registers require complete power cycle before it takes in effect. Changing these registers under normal operation is considered an illegal operation. Register modification is NOT allowed in Secure Mode.
0x20 - 0x2D	Host Region	Registers are copied from DIMM Vender Region setting at power-on.

8.3 Host Region Register Map

Register	Attribute	Description
0x00	RV	R00 [7:0] - Reserved
0x01	RV	R01 [7:0] - Reserved
0x02	RV	R02 [7:0] - Reserved
0x03	RV	R03 [7:0] - Reserved
0x04	ROE	R04 [7] Global Error Count R04 [6] Global Error Log - Buck OV or UV R04 [5] Global Error Log - VIN_Bulk OV R04 [4] Global Error Log - Critical Temperature R04 [3:0] Reserved
0x05	ROE	R05 [7] Reserved R05 [6] Power-On Reset - SWA Power Not Good

Register	Attribute	Description
		R05 [5] Reserved R05 [4:3] Power-On Reset - SWB & SWC Power Not Good R05 [2:0] Power-On Reset - High Level Error Log Code
0x06	ROE	R06 [7] PMIC Power-On - SWA Under-Voltage Lockout R06 [6] Reserved R06 [5:4] PMIC Power-On - SWB & SWC Under-Voltage Lockout R06 [3] PMIC Power-On - SWA Over-Voltage R06 [2] Reserved R06 [1:0] PMIC Power-On - SWB & SWC Over-Voltage
0x07	RV	R07 [7:0] Reserved
0x08	RO	R08 [7] Reserved R08 [6] Critical Temperature Shutdown Status R08 [5] SWA Output Power Good Status R08 [4] Reserved R08 [3:2] SWB, SWC Output Power Good Status R08 [1] Reserved R08 [0] VIN_Bulk Input Over-Voltage Status
0x09	RO	R09 [7] PMIC High Temperature Warning Status R09 [6] Reserved R09 [5] VOUT_1.8V Output Power Good Status R09 [4] Reserved R09 [3] SWA High Output Current Consumption Warning Status R09 [2] Reserved R09 [1:0] SWB, SWC High Output Current Consumption Warning Status
0x0A	RO	R0A [7] SWA Output Over-Voltage Status R0A [6] Reserved R0A [5:4] SWB, SWC Output Over-Voltage Status R0A [3] PEC Error Status R0A [2] Parity Error Status R0A [1] IBI Status R0A [0] Reserved
0x0B	RO	R0B [7] SWA Output Current Limiter Warning Status R0B [6] Reserved R0B [5:4] SWB, SWC Output Current Limiter Warning Status R0B [3] SWA Output Under-Voltage Lockout Status R0B [2] Reserved R0B [1:0] SWB, SWC Output Current Limiter Warning Status
0x0C	RO	R0C [7:0] SWA Output Current or Power or Total Output Power Measurement
0x0D	RV	R0D [7:0] Reserved
0x0E	RO	R0E [7:6] Reserved R0E [5:0] SWB Output Current or Power Measurement
0x0F	RO	R0F [7:6] Reserved

Register	Attribute	Description
		R0F [5:0] SWC Output Current or Power Measurement
0x10	1O	R10 [7:6] Reserved R10 [5] Clear SWA Output Power Good Status R10 [4] Reserved R10 [3:2] Clear SWB, SWC Output Power Good Status R10 [1] Reserved R10 [0] Clear VIN_Bulk Input Over-Voltage Status
0x11	1O	R11 [7] Clear PMIC High Temperature Warning Status R11 [6] Reserved R11 [5] Clear VOUT_1.8V Output Power Good Status R11 [4] Reserved R11 [3] Clear SWA High Output Current Consumption Warning Status R11 [2] Reserved R11 [1:0] Clear SWB, SWC High Output Current Consumption Warning Status
0x12	1O	R12 [7] Clear SWA Output Over-Voltage Status R12 [6] Reserved R12 [5:4] Clear SWB, SWC Output Over-Voltage Status R12 [3] Clear PEC Error R12 [2] Clear Parity Error R12 [1:0] Reserved
0x13	1O	R13 [7:4] Clear SWA Output Current Limiter Warning Status R13 [6] Reserved R13 [5:4] Clear SWB, SWC Output Current Limiter Warning Status R13 [3] Clear SWA Output Under-Voltage Lockout Status R13 [2] Reserved R13 [1:0] Clear SWB, SWC Output Under-Voltage Lockout Status
0x14	RW	R14 [7:3] Reserved R14 [2] Clear VOUT_1.0V Output Power Good Status R14 [1] Reserved R14 [0] Clear Global Status
0x15	RW	R15 [7:6] Reserved R15 [5] Mask SWA Output Power Good Status R15 [4] Reserved R15 [3:2] Mask SWB, SWC Output Power Good Status R15 [1] Reserved R15 [0] Mask VIN_Bulk Input Over-Voltage Status
0x16	RW	R16 [7] Mask PMIC High Temperature Warning Status R16 [6] Reserved R16 [5] Mask VOUT_1.8V Output Power Good Status R16 [4] Reserved R16 [3:0] Mask SWA High Output Current Consumption Warning Status R16 [2] Reserved

Register	Attribute	Description
		R16 [1:0] Mask SWB, SWC High Output Current Consumption Warning Status
0x17	RW	R17 [7] Mask SWA Output Over-Voltage R17 [6] Reserved R17 [5:4] Mask SWB, SWC Output Over-Voltage R17 [3] Mask PEC Error Status R17 [2] Mask Parity Error Status R17 [1:0] Reserved
0x18	RW	R18 [7] Mask SWA Output Current Limiter Warning Status R18 [6] Reserved R18 [5:4] Mask SWB, SWC Output Current Limiter Warning Status R18 [3] Mask SWA Output Under-Voltage Lockout Status R18 [2] Reserved R18 [3:0] Mask SWB, SWC Output Under-Voltage Lockout Status
0x19	RW	R19 [7:3] Reserved R19 [2] Mask VOUT_1.0 V Output Power Good Status R19 [1:0] Reserved
0x1A	RW	R1A [7:5] Reserved R1A [4] Quiescent Power State Entry Enable R1A [3] Reserved R1A [2] VOUT_1.8 V Power Good Threshold Voltage R1A [1] Output Power Select R1A [0] VOUT_1.0 V Power Good Threshold Voltage
0x1B	RW	R1B [7] VIN_Bulk Input Over-Voltage Threshold R1B [6] Current or Power Meter Select R1B [5] Reserved R1B [4] Global Mask PWR_GOOD Output Pin R1B [3] GSI_n Pin Enable R1B [2:0] PMIC High Temperature Warning Threshold
0x1C	RV	R1C [7:0] Reserved
0x1D	RV	R1D [7:0] Reserved
0x1E	RV	R1E [7:0] Reserved
0x1F	RV	R1F [7:0] Reserved
0x20	RW	R20 [7:6] SWA Output Current Limiter Warning Threshold R20 [5:4] Reserved R20 [3:2] SWB Output Current Limiter Warning Threshold R20 [1:0] SWC Output Current Limiter Warning Threshold
0x21	RW	R21 [7:1] SWA Voltage Setting R21 [0] Reserved
0x22	RW	R22 [7:6] SWA Power Good High-Side Threshold R22 [5:4] SWA Over-Voltage Threshold R22 [3:2] SWA Under-Voltage Lockout Threshold R22 [1:0] SWA Soft-Stop Time

Register	Attribute	Description
0x23	RV	R23 [7:0] Reserved
0x24	RV	R24 [7:0] Reserved
0x25	RW	R25 [7:1] SWB Voltage Setting R25 [0] SWB Power Good Low-Side Threshold
0x26	RW	R26 [7:6] SWB Power Good High-Side Threshold R26 [5:4] SWB Over-Voltage Threshold R26 [3:2] SWB Under-Voltage Lockout Threshold R26 [1:0] SWB Soft-Stop Time
0x27	RW	R27 [7:1] SWC Voltage Setting R27 [0] Reserved
0x28	RW	R28 [7:6] SWC Power Good High-Side Threshold R28 [5:4] SWC Over-Voltage Threshold R28 [3:2] SWC Under-Voltage Lockout Threshold R28 [1:0] SWC Soft-Stop Time
0x29	RW	R29 [7:6] SWA Mode Select R29 [5:4] SWA Switching Frequency R29 [3:0] Reserved
0x2A	RW	R2A [7:6] SWB Mode Select R2A [5:4] SWB Switching Frequency R2A [3:2] SWC Mode Select R2A [1:0] SWC Switching Frequency
0x2B	RW	R2B [7:6] VOUT_1.8 V LDO Setting R2B [5:3] Reserved R2B [2:1] VOUT_1.0 V LDO Setting R2B [0] Reserved
0x2C	RW	R2C [7:5] SWA Soft-Start Time R2C [4:0] Reserved
0x2D	RW	R2D [7:5] SWB Soft-Start Time R2D [4] Reserved R2D [3:1] SWC Soft-Start Time R2D [0] Reserved
0x2E	RW	R2E [7:3] Reserved R2E [2:0] PMIC Shutdown temperature threshold
0x2F	RW	R2F [7] Reserved R2F [6] SWA Enable R2F [5] Reserved R2F [4:3] SWB, SWC Enable R2F [2] Secure or Programmable Mode Select R2F [1:0] Mask Bits Register Control
0x30	RW	R30 [7] ADC Enable R30 [6:3] ADC Select R30 [2] Reserved R30 [1:0] ADC Register Update Frequency

Register	Attribute	Description
0x31	RO	R31 [7:0] ADC Read Out
0x32	RW, RO[6]	R32 [7] VR Enable R32 [6] Management Interface Selection R32 [5] PWR_GOOD Signal IO Type R32 [4:3] PMIC Power Good Output Signal Control R32 [2:0] Reserved
0x33	RO	R33 [7:5] Temperature Measurement R33 [4:3] Reserved R33 [2] VOUT_1.0V Output Power Good Status R33 [1:0] Reserved
0x34	RO	R34 [7] PEC Enable R34 [6] IBI Enable R34 [5] Parity Disable R34 [4] Reserved R34 [3:1] HID_CODE R34 [0] Reserved
0x35	RW	R35 [7] Error Injection Enable R35 [6:4] Rail Selection R35 [3] Over and Under-Voltage Select R35 [2:0] Misc. Error Injection Type
0x36	RV	R36 [7:0] Reserved
0x37	WO	R37 [7:0] Password Lower Byte 0
0x38	WO	R38 [7:0] Password Lower Byte 1
0x39	RW	R39 [7:0] Command Codes
0x3A	RW	R3A [7] Reserved R3A [6] Default Read Address Pointer Enable R3A [5:4] Default Read Address Pointer Selection R3A [3:2] Burst Length for Default Read Address Pointer Mode in PEC Enabled Mode R3A [1:0] Reserved
0x3B	ROE	R3B [7:6] Reserved R3B [5:4] Major Revision ID R3B [3:1] Minor Revision ID R3B [0] PMIC Current Capability
0x3C	ROE	R3C [7:0] VENDOR_ID_BYTE0
0x3D	ROE	R3D [7:0] VENDOR_ID_BYTE1
0x3E	RV	R3E [7:0] Reserved
0x3F	RV	R3F [7:0] Reserved

8.4 DIMM Region Register Map

Register	Attribute	Description
0x40	RWPE	R40 [7:0] Power-On Sequence - Configuration 0
0x41	RWPE	R41 [7:0] Power-On Sequence - Configuration 1

Register	Attribute	Description
0x42	RWPE	R42 [7:0] Power-On Sequence - Configuration 2
0x43	RV	R43 [7:0] Reserved
0x44	RV	R44 [7:0] Reserved
0x45	RWPE	R45 [7:1] SWA Voltage Setting R45 [0] SWA Power Good Low-Side Threshold
0x46	RWPE	R46 [7:6] Reserved R46 [5:4] SWA Over-Voltage Threshold R46 [3:2] SWA Under-Voltage Lockout Threshold R46 [1:0] SWA Soft-Stop Time
0x47	RV	R47 [7:0] Reserved
0x48	RV	R48 [7:0] Reserved
0x49	RWPE	R49 [7:1] SWB Voltage Setting R49 [0] SWB Power Good Low-Side Threshold
0x4A	RWPE	R4A [7:6] Reserved R4A [5:4] SWB Over-Voltage Threshold R4A [3:2] SWB Under-Voltage Lockout Threshold R4A [1:0] SWB Soft-Stop Time
0x4B	RWPE	R4B [7:1] SWC Voltage Setting R4B [0] SWC Power Good Low-Side Threshold
0x4C	RWPE	R4C [7:6] Reserved R4C [5:4] SWC Over-Voltage Threshold R4C [3:2] SWC Under-Voltage Lockout Threshold R4C [1:0] SWC Soft-Stop Time
0x4D	RWPE	R4D [7:6] SWA Mode Select R4D [5:4] SWA Switching Frequency R4D [3:0] Reserved
0x4E	RWPE	R4E [7:6] SWB Mode Select R4E [5:4] SWB Switching Frequency R4E [3:2] SWC Mode Select R4E [1:0] SWC Switching Frequency
0x4F	RWPE	R4F [7:1] Reserved R4F [0] SWA and SWB Single or Dual Phase Regulator Mode Select
0x50	RWPE	R50 [7:6] SWA Output Current Limiter Warning Threshold R50 [5:4] Reserved R50 [3:2] SWB Output Current Limiter Warning Threshold R50 [1:0] SWC Output Current Limiter Warning Threshold
0x51	RWPE	R51 [7:6] VOUT_1.8V LDO Output Voltage Setting R51 [5:3] Reserved R51 [2:1] VOUT_1.0V LDO Voltage Setting R51 [0] Reserved
0x52 – 0x57	RV	R52 [7:0] - R57 [7:0] Reserved
0x58	RWPE	R58 [7:0] Power Off Sequence - Configuration 0

Register	Attribute	Description
0x59	RWPE	R59 [7:0] Power Off Sequence - Configuration 1
0x5A	RWPE	R5A [7:0] Power Off Sequence - Configuration 2
0x5B	RV	R5B [7:0] Reserved
0x5C	RV	R5C [7:0] Reserved
0x5D	RWPE	R5D [7:5] SWA Soft-Start Time R5D [4:0] Reserved
0x5E	RWPE	R5E [7:5] SWB Soft-Start Time R5E [4] Reserved R5E [3:1] SWC Soft-Start Time R5E [0] Reserved
R5F-R6F	RV	R5F [7:0] to R6F [7:0] Reserved

8.5 Register Definition

8.5.1 Host Region Registers

R00 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R00 [7:0]: Reserved

R01 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R01 [7:0]: Reserved

R02 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R02 [7:0]: Reserved

R03 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R03 [7:0]: Reserved

R04 - Global Error Log			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R04 [7]: GLOBAL_ERROR_COUNT Global Error Count Since Last Erase Operation 0 = No Error or Only 1 Error Since Last Erase Operation 1 = > 1 Error Count since last Erase Operation
6	ROE	0	R04 [6]: GLOBAL_ERROR_LOG_BUCK_OV_OR_UV Global Error Log History for Buck Regulator Output Over-Voltage or Under- Voltage 0 = No Error Occurred 1 = Error Occurred

R04 - Global Error Log			
Bits	**Attribute**	**Default**	**Description**
5	ROE	0	R04 [5]: GLOBAL_ERROR_LOG_VIN_BULK_OVER_VOTLAGE Global Error Log History for VIN_BULK Over-Voltage 0 = No Error Occurred 1 = Error Occurred
4	ROE	0	R04 [4]: GLOBAL_ERROR_LOG_CRITICAL_TEMPERATURE Global Error Log History for Critical Temperature 0 = No Error Occurred 1 = Error Occurred
3:0	RV	0	R04 [3:0]: Reserved

R05 - Power Good Signal Control			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R05 [7]: Reserved
6	ROE	0	R05 [6]: SWA_POWER_GOOD PMIC Power-On - SWA Power Not Good 0 = Normal Power-On 1 = SWA Power Not Good
5	RV	0	R05 [5]: Reserved
4	ROE	0	R05 [4]: SWB_POWER_GOOD PMIC Power-On - SWB Power Not Good 0 = Normal Power-On 1 = SWB Power Not Good
3	ROE	0	R05 [3]: SWC_POWER_GOOD PMIC Power-On - SWC Power Not Good 0 = Normal Power-On 1 = SWC Power Not Good
2:0	ROE	0	R05 [2:0]: PMIC_ERROR_LOG PMIC Power-On - High Level Status Bit to Indicate Last Known Power Cycle or System Reset 000 = Normal Power-On 001 = Reserved 010 = Buck Regulator Output Over or Under-Voltage 011 = Critical Temperature 100 = VIN_Bulk Input Over-Voltage 101 = Reserved 110 = Reserved 111 = Reserved

R06 - UVLO Function Control			
Bits	**Attribute**	**Default**	**Description**
7	ROE	0	R06 [7]: SWA_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWA Under-Voltage Lockout 0 = Normal Power-On 1 = Power-On - SWA Under-Voltage Lockout
6	RV	0	R06 [6]: Reserved
5	ROE	0	R06 [5]: SWB_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWB Under-Voltage Lockout 0 = Normal Power-On 1 = SWB Under-Voltage Lockout
4	ROE	0	R06 [4]: SWC_UNDER_VOLTAGE_LOCKOUT PMIC Power-On - SWC Under-Voltage Lockout 0 = Normal Power-On 1 = SWC Under-Voltage Lockout
3	ROE	0	R06 [3]: SWA_OVER_VOLTAGE PMIC Power-On - SWA Over-Voltage 0 = Normal Power-On 1 = SWA Over-Voltage
2	RV	0	R06 [2]: Reserved
1	ROE	0	R06 [1]: SWB_OVER_VOLTAGE PMIC Power-On - SWB Over-Voltage 0 = Normal Power-On 1 = SWB Over-Voltage
0	ROE	0	R06 [0]: SWC_OVER_VOLTAGE PMIC Power-On - SWC Over-Voltage 0 = Normal Power-On 1 = SWC Over-Voltage

R07 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R07 [7:0]: Reserved

R08 - Power Good Status			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R08 [7]: Reserved
6	RO	0	R08 [6]: CRITICAL_TEMP_SHUTDOWN_STATUS Critical Temperature Shutdown Status 0 = No Critical Temperature Shutdown 1 = Critical Temperature Shutdown
5	RO	0	R08 [5]: SWA_OUTPUT_POWER_GOOD_STATUS Switch Node A Output Power Good Status 0 = Power Good

R08 - Power Good Status			
Bits	**Attribute**	**Default**	**Description**
			1 = Power Not Good
4	RO	0	R08 [4]: Reserved
3	RO	0	R08 [3]: SWB_OUTPUT_POWER_GOOD_STATUS Switch Node B Output Power Good Status 0 = Power Good 1 = Power Not Good
2	RO	0	R08 [2]: SWC_OUTPUT_POWER_GOOD_STATUS Switch Node C Output Power Good Status 0 = Power Good 1 = Power Not Good
1	RO	0	R08 [1]: Reserved
0	RO	0	R08 [0]: VIN_BULK_INPUT_OVER_VOLTAGE_STATUS VIN_BULK Input Supply Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage

R09 - High Temperature and Current Warning Status			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R09 [7]: PMIC_HIGH_TEMP_WARNING_STATUS PMIC High Temperature Warning Status 0 = Temperature Below the Warning Threshold 1 = Temperature Exceeded the Warning Threshold
6	RV	0	R09 [6]: Reserved
5	RO	0	R09 [5]: VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS VOUT_1.8V LDO Output Power Good Status2 0 = Power Good 1 = Power Not Good
4	RV	0	R09 [4]: Reserved
3	RO	0	R09[3]: SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATU S Switch Node A High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
2	RV	0	R09 [2]: Reserved
1	RO	0	R09 [1]: SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATU S Switch Node B High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning
0	RO	0	R09 [0]: SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATU S Switch Node C High Output Current Consumption Warning Status 0 = No High Current Consumption Warning 1 = High Current Consumption Warning

R0A - OVP and Error Status			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0A [7]: SWA_OUTPUT_OVER_VOLTAGE_STATUS Switch Node A Output Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
6	RV	0	R0A [6]: Reserved
5	RO	0	R0A [5]: SWB_OUTPUT_OVER_VOLTAGE_STATUS Switch Node B Output Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
4	RO	0	R0A [5]: SWC_OUTPUT_OVER_VOLTAGE_STATUS Switch Node C Output Over-Voltage Status 0 = No Over-Voltage 1 = Over-Voltage
3	RO	0	R0A [3]: PEC_ERROR_STATUS Packet Error Code Status 0 = No PEC Error 1 = PEC Error
2	RO	0	R0A [2]: PARITY_ERROR_STATUS T Bit Parity Error Status 0 = No Parity Error 1 = Parity Error
1	RO	0	R0A [1]: IBI_STATUS In Band Interrupt Status 0 = No Pending IBI 1 = Pending IBI
0	RV	0	R0A [0]: Reserved

R0B - Current Limit and UVLO Status			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R0B [7]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node A Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
6	RV	0	R0B [6]: Reserved
5	RO	0	R0B [5]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node B Output Current Limiter Warning Status 0 = No Current Limiter Event 1 = Current Limiter Event
4	RO	0	R0B [4]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Switch Node C Output Current Limiter Warning Status 0 = No Current Limiter Event

R0B - Current Limit and UVLO Status			
Bits	**Attribute**	**Default**	**Description**
			1 = Current Limiter Event
3	RO	0	R0B [3]: SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node A Output Under-Voltage Lockout Status 0 = No Under-Voltage Lockout 1 = Under-Voltage Lockout
2	RV	0	R0B [2]: Reserved
1	RO	0	R0B [1]: SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node B Output Under-Voltage Lockout Status 0 = No Under-Voltage Lockout 1 = Under-Voltage Lockout
0	RO	0	R0B [0]: SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Switch Node C Output Under-Voltage Lockout Status 0 = No Under-Voltage Lockout 1 = Under-Voltage Lockout

R0C - SWA Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R0C [7:0]: SWA_OUTPUT_CURRENT_POWER_MEASUREMENT If Register R1A [1] = 0, Switch Node A Output Current or Output Power Measurement. 0000 0000 = Undefined 0000 0001 = 0.125A or 125mW 0000 0010 = 0.25A or 250mW 0000 0011 = 0.375A or 375mW 0000 0100 = 0.5A or 500mW 0000 0101 = 0.625A or 625mW 0000 0110 = 0.75A or 750mW 0000 0111 = 0.875A or 875mW 0000 1000 = 1.0A or 1000mW 0000 1001 = 1.125A or 1125mW .. .. 0011 0111 = 6.875A or 6875mW 0011 1000 = 7.0A or 7000mW 0011 1001 = 7.125A or 7125mW 0011 1010 = 7.25A or 7250mW 0011 1011 = 7.375A or 7375mW 0011 1100 = 7.5A or 7500mW 0011 1101 = 7.625A or 7625mW 0011 1110 = 7.75A or 7750mW 0011 1111 >= 7.875A or 7875mW

R0C - SWA Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
			All other encodings are reserved. If Register R1A [1] = 1, Sum of power measurement for Switch Outputs SWA, SWB and SWC. 0000 0000 = Undefined 0000 0001 = 125mW 0000 0010 = 250mW 0000 0011 = 375mW 0000 0100 = 500mW ... ... 1111 1100 = 31500mW 1111 1101 = 31625mW 1111 1110 = 31750mW 1111 1111 ≧ 31875mW

R0D - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R0D [7:0]: Reserved

R0E - SWB Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0E [7:6]: Reserved
5:0	RO	0	R0E [5:0]: SWB_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node B Output Current or Output Power Measurement. 000000 = Undefined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW 001010 = 1.25A or 1250mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW

R0E - SWB Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
			111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 ≧ 7.875A or 7875mW

R0F - SWC Current & Power Measurement			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R0F [7:6]: Reserved
5:0	RO	0	R0F [5:0]: SWC_OUTPUT_CURRENT_POWER_MEASUREMENT Switch Node C Output Current or Output Power Measurement. 000000 = Undefined 000001 = 0.125A or 125mW 000010 = 0.25A or 250mW 000011 = 0.375A or 375mW 000100 = 0.5A or 500mW 000101 = 0.625A or 625mW 000110 = 0.75A or 750mW 000111 = 0.875A or 875mW 001000 = 1.0A or 1000mW 001001 = 1.125A or 1125mW 001010 = 1.25A or 1250mW ... 110111 = 6.875A or 6875mW 111000 = 7.0A or 7000mW 111001 = 7.125A or 7125mW 111010 = 7.25A or 7250mW 111011 = 7.375A or 7375mW 111100 = 7.5A or 7500mW 111101 = 7.625A or 7625mW 111110 = 7.75A or 7750mW 111111 ≧ 7.875A or 7875mW

R10 - Power Good Clear			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R10 [7:6]: Reserved
5	1O	0	R10 [5]: CLEAR_SWA_OUTPUT_POWER_GOOD_STATUS Clear SWA Output Power Good Status. 1 = Clear “Register R08” [5]
4	RV	0	R10 [4]: Reserved
3	1O	0	R10 [3]: CLEAR_SWB_OUTPUT_POWER_GOOD_STATUS

R10 - Power Good Clear			
Bits	**Attribute**	**Default**	**Description**
			Clear SWB Output Power Good Status. 1 = Clear “Register R08” [3]
2	1O	0	R10 [2]: CLEAR_SWC_OUTPUT_POWER_GOOD_STATUS Clear SWC Output Power Good Status. 1 = Clear “Register R08” [2]
1	RV	0	R10 [1]: Reserved
0	1O	0	R10 [0]: CLEAR_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Clear VIN_BULK Input Supply Over-Voltage Status. 1 = Clear “Register R08” [0]

R11 - High Temperature and Current Warning Status Clear			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R11 [7]: CLEAR_PMIC_HIGH_TEMP_WARNING_STATUS Clear PMIC High Temperature Warning Status. 1 = Clear “Register R09” [7]
6	RV	0	R11 [6]: Reserved
5	1O	0	R11 [5]: CLEAR_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.8V Output Power Good Status 1 = Clear “Register R09” [5]
4	RV	0	R11 [4]: Reserved
3	1O	0	R11 [3]: CLEAR_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node A High Output Current Consumption Warning Status. 1 = Clear “Register R09” [3]
2	RV	0	R11 [2]: Reserved
1	1O	0	R11 [1]: CLEAR_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node B High Output Current Consumption Warning Status. 1 = Clear “Register R09” [1]
0	1O	0	R11 [0]: CLEAR_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_WARNING_STATUS Clear Switch Node C High Output Current Consumption Warning Status. 1 = Clear “Register R09” [0]

R12 - OVP Status Clear			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R12 [7]: CLEAR_SWA_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node A Output Over-Voltage Status. 1 = Clear “Register R0A” [7]
6	RV	0	R12 [6]: Reserved
5	1O	0	R12 [5]: CLEAR_SWB_OUTPUT_OVER_VOLTAGE_STATUS

R12 - OVP Status Clear			
Bits	**Attribute**	**Default**	**Description**
			Clear Switch Node B Output Over-Voltage Status. 1 = Clear “Register R0A” [5]
4	1O	0	R12 [4]: CLEAR_SWC_OUTPUT_OVER_VOLTAGE_STATUS Clear Switch Node C Output Over-Voltage Status. 1 = Clear “Register R0A” [4]
3	1O	0	R12 [3]: CLEAR_PER_ERROR_STATUS Clear PEC Error Status. 1 = Clear “Register 0x0A” [3]
2	1O	0	R12 [2]: CLEAR_PARITY_ERROR_STATUS Clear Parity Error Status. 1 = Clear “Register 0x0A” [2]
1:0	RV	0	R12 [1:0]: Reserved

R13 - Current Limit Status Clear			
Bits	**Attribute**	**Default**	**Description**
7	1O	0	R13 [7]: CLEAR_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node A Output Current Limiter Warning Status. 1 = Clear “Register R0B” [7]
6	RV	0	R13 [6]: Reserved
5	1O	0	R13 [5]: CLEAR_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node B Output Current Limiter Warning Status. 1 = Clear “Register R0B” [5]
4	1O	0	R13 [4]: CLEAR_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Clear Switch Node C Output Current Limiter Warning Status. 1 = Clear “Register R0B” [4]
3	1O	0	R13 [3]: CLEAR_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node A Output Under-Voltage Lockout Status. 1 = Clear “Register R0B” [3]
2	RV	0	R13 [2]: Reserved
1	1O	0	R13 [1]: CLEAR_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node B Output Under-Voltage Lockout Status. 1 = Clear “Register R0B” [1]
0	1O	0	R13 [0]: CLEAR_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Clear Switch Node C Output Under-Voltage Lockout Status. 1 = Clear “Register R0B” [0]

R14 - Global Clear Status			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R14 [7:3]: Reserved
2	1O	0	R14 [2]: CLEAR_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Clear VOUT_1.0V Output Power Good Status.

R14 - Global Clear Status			
Bits	**Attribute**	**Default**	**Description**
			1 = Clear “Register R33” [2]
1	RV	0	R14 [1]: Reserved
0	1O	0	R14 [0]: GLOBAL_CLEAR_STATUS Clear all status bits. 1 = Clear all status bits

R15 - Power Good Status Mask			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R15 [6]: Reserved
5	RW	1	R15 [5]: MASK_SWA_OUTPUT_POWER_GOOD_STATUS Mask SWA Output Power Good Status Event1. 0 = Do Not Mask SWA Output Power Good Status Event 1 = Mask SWA Output Power Good Status Event
4	RV	0	R15 [4]: Reserved
3	RW	1	R15 [3]: MASK_SWB_OUTPUT_POWER_GOOD_STATUS Mask SWB Output Power Good Status Event1,2. 0 = Do Not Mask SWB Output Power Good Status Event 1 = Mask SWB Output Power Good Status Event
2	RW	1	R15 [2]: MASK_SWC_OUTPUT_POWER_GOOD_STATUS Mask SWC Output Power Good Status Event1. 0 = Do Not Mask SWC Output Power Good Status Event 1 = Mask SWC Output Power Good Status Event
1	RV	0	R15 [1]: Reserved
0	RW	0	R15 [0]: MASK_VIN_BULK_INPUT_OVER_VOLTAGE_STATUS Mask VIN_Bulk Input Supply Over-Voltage Status Event. 0 = Do Not Mask VIN_Bulk Input Supply Over-Voltage Status Event 1 = Mask VIN_Bulk Input Supply Over-Voltage Status Event

R16 - High Temperature and Current Warning Status Mask			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R16 [7]: MASK_PMIC_HIGH_TEMP_WARNING_STATUS Mask PMIC High Temperature Warning Status Event. 0 = Do Not Mask PMIC High Temperature Warning Status Event 1 = Mask PMIC High Temperature Warning Status Event
6	RV	0	R16 [6]: Reserved
5	RW	1	R16 [5]: MASK_VOUT_1.8V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.8V Output Power Good Status Event. 0 = Do Not Mask 1.8V Output Power Good Status Event 1 = Mask 1.8V Output Power Good Status Event
4	RV	0	R16 [4]: Reserved
3	RW	0	R16 [3]: MASK_SWA_HIGH_OUTPUT_CURRENT_CONSUMPTION_

R16 - High Temperature and Current Warning Status Mask			
Bits	**Attribute**	**Default**	**Description**
			WARNING_STATUS Mask Switch Node A High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Consumption Warning Status Event 1 = Mask Switch Node A Output Current Consumption Warning Status Event
2	RV	0	R16 [2]: Reserved
1	RW	0	R16 [1]: MASK_SWB_HIGH_OUTPUT_CURRENT_CONSUMPTION_ WARNING_STATUS Mask Switch Node B High Output Current Consumption Warning Status Event 0 = Do Not Mask Switch Node B Output Current Consumption Warning Status Event 1 = Mask Switch Node B Output Current Consumption Warning Status Event
0	RW	0	R16 [0]: MASK_SWC_HIGH_OUTPUT_CURRENT_CONSUMPTION_ WARNING_STATUS Mask Switch Node C High Output Current Consumption Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Consumption Warning Status Event 1 = Mask Switch Node C Output Current Consumption Warning Status Event

R17 - Over Voltage and Error Status Mask			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R17 [7]: MASK_SWA_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node A Output Over-Voltage Status Event. 0 = Do Not Mask Switch Node A Output Over-Voltage Status Event 1 = Mask Switch Node A Output Over-Voltage Status Event
6	RV	0	R17 [6]: Reserved
5	RW	0	R17 [5]: MASK_SWB_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node B Output Over-Voltage Status Event2. 0 = Do Not Mask Switch Node B Output Over-Voltage Status Event 1 = Mask Switch Node B Output Over-Voltage Status Event
4	RW	0	R17 [4]: MASK_SWC_OUTPUT_OVER_VOLTAGE_STATUS Mask Switch Node C Output Over-Voltage Status Event. 0 = Do Not Mask Switch Node C Output Over-Voltage Status Event 1 = Mask Switch Node C Output Over-Voltage Status Event
3	RW	0	R17 [3]: MASK_PEC_ERROR_STATUS Mask PEC Error Event for GSI_n output Only 0 = Do Not Mask PEC Error Status Event 1 = Mask PEC Error Status
2	RW	0	R17 [2]: MASK_PARITY_ERROR_STATUS Mask Parity Error Event for GSI_n output Only 0 = Do Not Mask Parity Error Status Event

R17 - Over Voltage and Error Status Mask			
Bits	**Attribute**	**Default**	**Description**
			1 = Mask Parity Error Status
1:0	RV	0	R17 [1:0]: Reserved

R18 - Current Limit and UVLO Status Mask			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R18 [7]: MASK_SWA_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node A Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node A Output Current Limiter Warning Status Event 1 = Mask Switch Node A Output Current Limiter Warning Status Event
6	RV	0	R18 [6]: Reserved
5	RW	0	R18 [5]: MASK_SWB_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node B Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node B Output Current Limiter Warning Status Event 1 = Mask Switch Node B Output Current Limiter Warning Status Event
4	RW	0	R18 [4]: MASK_SWC_OUTPUT_CURRENT_LIMITER_WARNING_STATUS Mask Switch Node C Output Current Limiter Warning Status Event. 0 = Do Not Mask Switch Node C Output Current Limiter Warning Status Event 1 = Mask Switch Node C Output Current Limiter Warning Status Event
3	RW	0	R18 [3]: MASK_SWA_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node A Output Under-Voltage Lockout Status Event. 0 = Do Not Mask Switch Node A Output Under-Voltage Lockout Status Event 1 = Mask Switch Node A Output Under-Voltage Lockout Status Event
2	RV	0	R18 [2]: Reserved
1	RW	0	R18 [1]: MASK_SWB_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node B Output Under-Voltage Lockout Status Event3. 0 = Do Not Mask Switch Node B Output Under-Voltage Lockout Status Event 1 = Mask Switch Node B Output Under-Voltage Lockout Status Event
0	RW	0	R18 [0]: MASK_SWC_OUTPUT_UNDER_VOLTAGE_LOCKOUT_STATUS Mask Switch Node C Output Under-Voltage Lockout Status Event. 0 = Do Not Mask Switch Node C Output Under-Voltage Lockout Status Event 1 = Mask Switch Node C Output Under-Voltage Lockout Status Event

R19 – LDO 1.0V Power Good Status Mask			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R19 [7:3]: Reserved
2	RW	1	R19 [2]: MASK_VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS Mask VOUT_1.0V Output Power Good Status Event. 0 = Do Not Mask 1.0V Output Power Good Status Event 1 = Mask 1.0V Output Power Good Status Event
1:0	RV	0	R19 [1:0]: Reserved

R1A - Quiescent State			
Bits	**Attribute**	**Default**	**Description**
7:5	RV	000	R1A [7:5]: Reserved
4	RW	0	R1A [4]: QUIESCENT_STATE_EN PMIC Quiescent State Entry Enable 0 = Disable 1 = Enable
3	RV	0	R1A [3]: Reserved
2	RW	0	R1A [2]: VOUT_1.8V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.8V LDO Output Threshold Voltage for Power Good Status 0 = 1.6V 1 = Reserved
1	RW	0	R1A [1]: OUTPUT_POWER_SELECT Switch Regulator Output Power Select 0 = Report Power Measurement for Each Rail in R0C, R0E & R0F 1 = Report Total Power Measurement of Each Rail in R0C
0	RW	0	R1A [0]: VLDO_1.0V_POWER_GOOD_THRESHOLD_VOLTAGE VOUT 1.0V LDO Output Threshold Voltage for Power Good Status 0 = -10% from the setting in “Register R51” [2:1] 1 = -15% from the setting in “Register R51” [2:1]

R1B - High Temperature Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R1B [7]: VIN_BULK_OVER_VOLTAGE_THRESHOLD VIN_Bulk Input Over-Voltage Threshold Setting For GSI_n Assertion 0 = 5.8 V 1 = Reserved
6	RW	0	R1B [6]: CURRENT_OR_POWER_METER_SELECT PMIC Output Regulator Measurement - Current or Power Meter 0 = Report Current Measurements in registers 1 = Report Power Measurements in registers
5	RV	0	R1B [5]: Reserved
4	RW	0	R1B [4]: GLOBAL_PWR_GOOD_PIN_STATUS_MASK Global Mask PWR_GOOD Output Pin 0 = Not Masked 1 = Masked
3	RW	0	R1B [3]: GSI_N_PIN_ENABLE Enable GSI_n Pin 0 = Disable GSI_n Pin 1 = Enable GSI_n Pin
2:0	RW	101	R1B [2:0]: PMIC_HIGH_TEMPERATURE_WARNING_THRESHOLD PMIC High Temperature Warning Threshold 000 = Reserved 001 = PMIC temperature ≥ 85ºC

R1B - High Temperature Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
			010 = PMIC temperature ≥ 95ºC 011 = PMIC temperature ≥ 105ºC 100 = PMIC temperature ≥ 115ºC 101 = PMIC temperature ≥ 125ºC 110 = PMIC temperature ≥ 135ºC 111 = Reserved

R1C - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1C [7:2]: SWA_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node A Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = > 0.125A 000010 = > 0.25A 000011 = > 0.375A 000100 = > 0.5A 000101 = > 0.625A 000110 = > 0.75A 000111 = > 0.875A 001000 = > 1.0A 001001 = > 1.125A ... ... 010111 = > 2.875A 011000 = > 3.0A 011001 = > 3.125A ... 110111 = > 6.875A 111000 = > 7.0A 111001 = > 7.125A 111010 = > 7.25A 111011 = > 7.375A 111100 = > 7.5A 111101 = > 7.625A 111110 = > 7.75A 111111 = > 7.875A
1:0	RV	0	R1C [1:0]: Reserved

R1D - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R1D [7:0]: Reserved

R1E - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1E [7:2]: SWB_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node B Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = > 0.125A 000010 = > 0.25A 000011 = > 0.375A 000100 = > 0.5A 000101 = > 0.625A 000110 = > 0.75A 000111 = > 0.875A 001000 = > 1.0A 001001 = > 1.125A ... 010111 = > 2.875A 011000 = > 3.0A ... 110111 = > 6.875A 111000 = > 7.0A 111001 = > 7.125A 111010 = > 7.25A 111011 = > 7.375A 111100 = > 7.5A 111101 = > 7.625A 111110 = > 7.75A 111111 = > 7.875A
1:0	RV	0	R1E [1:0]: Reserved

R1F - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:2	RW	011000	R1F [7:2]: SWC_OUTPUT_HIGH_CURRENT_CONSUMPTION_WARNING_THRESHOLD Switch Node C Output High Current Consumption Warning Threshold 000000 = Un-defined 000001 = > 0.125A 000010 = > 0.25A 000011 = > 0.375A

R1F - Reserved			
Bits	**Attribute**	**Default**	**Description**
			000100 = > 0.5A 000101 = > 0.625A 000110 = > 0.75A 000111 = > 0.875A 001000 = > 1.0A 001001 = > 1.125A ... 010111 = > 2.875A 011000 = > 3.0A 011001 = > 3.125A ... 110111 = > 6.875A 111000 = > 7.0A 111001 = > 7.125A 111010 = > 7.25A 111011 = > 7.375A 111100 = > 7.5A 111101 = > 7.625A 111110 = > 7.75A 111111 = > 7.875A
1:0	RV	0	R1F [1:0]: Reserved

R20 - Output Current Limit & High Current Consumption Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	00	R20 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, Ivalley_limit and Consumption Warning Threshold 00 = 5.0A 01 = 5.5A 10 = 6.0A 11 = Reserved
5:4	RV	00	R20 [5:4]: Reserved
3:2	RW	00	R20 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, valley_limit and Consumption Warning Threshold 00 = 5.0A 01 = 5.5A 10 = 6.0A 11 = Reserved
1:0	RW	11	R20 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING For COT Mode, valley_limit and Consumption Warning Threshold 00 = 0.5A

R20 - Output Current Limit & High Current Consumption Warning Threshold			
Bits	**Attribute**	**Default**	**Description**
			01 = 1.0A 10 = 1.5A 11 = 2.0A

R21 - SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R21 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RW	0	R21 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = -5% from the setting in “Register R21,” [7:1] 1 = -7.5% from the setting in “Register R21,” [7:1]

R22 - SWA Threshold and Soft stop time			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R22 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound level” For Power Good Status 00 = +5% from the setting in “Register R21,” [7:1] 01 = +7.5% from the setting in “Register R21,” [7:1] 10 = +10% from the setting in “Register R21,” [7:1] 11 = +3% from the setting in “Register R21,” [7:1]
5:4	RW	10	R22 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R21,” [7:1] 01 = +10% from the setting in “Register R21,” [7:1] 10 = +12.5% from the setting in “Register R21,” [7:1] 11 = +20% from the setting in “Register R21,” [7:1]
3:2	RW	00	R22 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under-Voltage Lockout Status 00 = -10% from the setting in “Register R21,” [7:1]

R22 - SWA Threshold and Soft stop time			
Bits	**Attribute**	**Default**	**Description**
			01 = -12.5% from the setting in “Register R21,” [7:1] 10 = -7.5% from the setting in “Register R21,” [7:1 11 = -20% from the setting in “Register R21,” [7:1]
1:0	RW	11	R22 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R23 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R23 [7:0]: Reserved

R24 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R24 [7:0]: Reserved

R25 - SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R25 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV ... 011 1100 = 1100mV ... 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RW	0	R25 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = -5% from the setting in “Register R25,” [7:1] 1 = -7.5% from the setting in “Register R25,” [7:1]

R26 - SWB Threshold and Soft stop time			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R26 [7:6]: SWB_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good

R26 - SWB Threshold and Soft stop time			
Bits	**Attribute**	**Default**	**Description**
			Status 00 = +5% from the setting in “Register R25,” [7:1] 01 = +7.5% from the setting in “Register R25,” [7:1] 10 = +10% from the setting in “Register R25,” [7:1] 11 = +3% from the setting in “Register R25,” [7:1]
5:4	RW	10	R26 [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R25,” [7:1] 01 = +10% from the setting in “Register R25,” [7:1] 10 = +12.5% from the setting in “Register R25,” [7:1] 11 = +20% from the setting in “Register R25,” [7:1]
3:2	RW	00	R26 [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node B Output Regulator Threshold For Under-Voltage Lockout Status 00 = -10% from the setting in “Register R25,” [7:1] 01 = -12.5% from the setting in “Register R25,” [7:1] 10 = -7.5% from the setting in “Register R25,” [7:1] 11 = -20% from the setting in “Register R25,” [7:1]
1:0	RW	11	R26 [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWB Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R27 - SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RW	0111100	R27 [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting 000 0000 = 1500mV 000 0001 = 1505mV 000 0010 = 1510mV ... 011 1100 = 1800mV ... 111 1101 = 2125mV 111 1110 = 2130mV 111 1111 = 2135mV
0	RW	0	R27 [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = -5% from the setting in “Register R27,” [7:1] 1 = -7.5% from the setting in “Register R27,” [7:1]

R28 - SWC Threshold and Soft stop time			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R28 [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R27” [7:1] 01 = +7.5% from the setting in “Register R27” [7:1] 10 = +10% from the setting in “Register R27” [7:1] 11 = +3% from the setting in “Register R27” [7:1]
5:4	RW	10	R28 [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R25” [7:1] 01 = +10% from the setting in “Register R25” [7:1] 10 = +12.5% from the setting in “Register R25” [7:1] 11 = +20% from the setting in “Register R27” [7:1]
3:2	RW	00	R28 [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under-Voltage Lockout Status 00 = -10% from the setting in “Register R25” [7:1] 01 = -12.5% from the setting in “Register R25” [7:1] 10 = -7.5% from the setting in “Register R27” [7:1] 11 = -20% from the setting in “Register R27” [7:1]
1:0	RW	11	R28 [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R29 - SWA FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R29 [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R29 [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency (Note) 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

R29 - SWA FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
3:0	RV	0000	R29 [3:0]: Reserved

R2A - SWB, SWC FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	10	R2A [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RW	00	R2A [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RW	10	R2A [3:2]: SWC_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RW	00	R2A [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

R2B - LDO Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:6	RW	01	R2B [7:6]: VOUT_1.8V _VOLTAGE_SETTING VLDO_1.8V Voltage Setting: 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5:3	RV	000	R2B [5:3]: Reserved
2:1	RW	01	R2B [2:1]: VOUT_1.0V _VOLTAGE_SETTING VLDO_1.0V Voltage Setting: 00 = 0.9V

R2B - LDO Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
			01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	R2B [0]: Reserved

R2C - SWA Soft Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2C [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4:0	RV	0	R2C [4:0]: Reserved

R2D - SWB, SWC Soft Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RW	001	R2D [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4	RV	0	R2D [4]: Reserved
3:1	RW	001	R2D [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	R2D [0]: Reserved

R2E - Shutdown Temp. Threshold			
Bits	**Attribute**	**Default**	**Description**
7:3	RV	0	R2E [7:3]: Reserved

R2E - Shutdown Temp. Threshold			
Bits	**Attribute**	**Default**	**Description**
2:0	RW	100	R2E [2:0]: PMIC_SHUTDOWN_TEMPERATURE_THRESHOLD PMIC Shutdown Temperature Threshold 000 = PMIC Temperature ≥ 105ºC 001 = PMIC Temperature ≥ 115ºC 010 = PMIC Temperature ≥ 125ºC 011 = PMIC Temperature ≥ 135ºC 100 = PMIC Temperature ≥ 145ºC 101 = Reserved 110 = Reserved 111 = Reserved

R2F - PMIC Configuration			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R2F [7]: Reserved
6	RW	0	R2F [6]: SWA_REGULATOR_CONTROL Disable SWA Regulator Output 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R2F [5]: Reserved
4	RW	0	R2F [4]: SWB_REGULATOR_CONTROL Disable SWB Regulator Output 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RW	0	R2F [3]: SWC_REGULATOR_CONTROL Disable SWC Regulator Output 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2	RW	0	R2F [2]: SECURE_MODE PMIC Mode Operation 0 = Secure Mode Operation 1 = Programmable Mode Operation
1:0	RW	10	R2F [1:0]: MASK_BITS_REGISTER_CONTROL Mask Bits Register Control 00 = Mask GSI_n Signal Only (PWR_GOOD Signal will assert) 01 = Mask PWR_GOOD Only (GSI_n signal will assert) 10 = Mask GSI_n and PWR_GOOD Signals (neither PWR_GOOD assert or GSI_n signal will assert) 11 = Reserved

R30 - ADC Enable			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R30 [7]: ADC_ENABLE Enable ADC (Analog to Digital Conversion) 0 = Disable 1 = Enable
6:3	RW	0	R30 [6:3]: ADC_SELECT Input Selection for ADC Readout 0000 = SWA Output Voltage 0001 = Reserved 0010 = SWB Output Voltage 0011 = SWC Output Voltage 0100 = Reserved 0101 = VIN_BULK Input Voltage 0110 = Reserved 0111 = Reserved 1000 = VOUT_1.8V Output Voltage 1001 = VOUT_1.0V Output Voltage All other encodings are reserved.
2	RV	0	R30 [2]: Reserved
1:0	RW	0	R30 [1:0]: ADC_REGISTER_UPDATE_FREQUENCY ADC Current or Power Measurement Update Frequency 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R31 - ADC Read			
Bits	**Attribute**	**Default**	**Description**
7:0	RO	0	R31 [7:0]: ADC_READ ADC Output Voltage Reading (Applies to SW[A:C], VOUT_1.8V, VOUT_1.0V) 0000 0000 = Undefined 0000 0001 = 15mV 0000 0010 = 30mV .. 1111 1111 >= 3825mV ADC Output Voltage Reading (Applies to VIN_BULK Input Voltage) 0000 0000 = Undefined 0000 0001 = 70mV 0000 0010 = 140mV .. 1111 1111 >= 17850mV

R32 - PMIC_EN & Mgmt Interface Selection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R32 [7]: VR_ENABLE PMIC Enable 0 = PMIC Disable 1 = PMIC Enable
6	RO	0	R32 [6]: MANAGEMENT_INTERFACE_SELECTION PMIC Management Bus Interface Protocol Selection 0 = I^2C Interface (Max speed 1MHZ) 1 = I^3C Basic Protocol
5	RW	0	R32 [5]: PWR_GOOD_IO_TYPE PMIC PWR_GOOD Output Signal Type 0 = Output only 1 = Input and Output
4:3	RW	00	R32 [4:3]: PMIC_PWR _OUTPUT_SIGNAL_CONTROL PMIC PWR_GOOD Output Signal Control 0x = PMIC controls PWR_GOOD on its own based on internal status 10 = PWR_GOOD Output Low 11 = PWR_GOOD Output Float
2:0	RV	0	R32 [2:0]: Reserved

R33 - Temp_Meas & LDO Status			
Bits	**Attribute**	**Default**	**Description**
7:5	RO	0	R33 [7:5]: TEMPERATURE_MEASUREMENT PMIC Temperature 000 < 85ºC (±5ºC) 001 = 85ºC (±5ºC) 010 = 95ºC (±5ºC) 011 = 105ºC (±5ºC) 100 = 115ºC (±5ºC) 101 = 125ºC (±5ºC) 110 = 135ºC (±5ºC) 111 > 140ºC (±5ºC)
4:3	RV	0	R33 [4]: Reserved
2	RO	0	R33 [2]: VOUT_1.0V_OUTPUT_POWER_GOOD_STATUS VOUT_1.0V LDO Output Power Good Status 0 = Power Good 1 = Power Not Good
1:0	RV	0	R33 [1:0]: Reserved

R34 - PEC/IBI/PARITY/HID_CODE			
Bits	**Attribute**	**Default**	**Description**
7	RO	0	R34 [7]: PEC_ENABLE

R34 - PEC/IBI/PARITY/HID_CODE			
Bits	**Attribute**	**Default**	**Description**
			Packet Error Code Enable (Applicable Only if R32 [6] = '1') 0 = Disable 1 = Enable
6	RO	0	R34 [6]: IBI_ENABLE In Band Interrupt Enable (Applicable Only if R32 [6] = '1') 0 = Disable 1 = Enable
5	RO	0	R34 [5]: PARITY_DISABLE T Bit Parity Code Disable (Applicable Only if R32 [6] = '1'.) 0 = Enable 1 = Disable
4	RV	0	R34 [4]: Reserved
3:1	RO	111	R34 [3:1]: HID_CODE PMIC's 3-bit HID Code 000 001 010 011 100 101 110 111
0	RV	0	R34 [0]: Reserved

R35 - Error Injection			
Bits	**Attribute**	**Default**	**Description**
7	RW	0	R35 [7]: ERROR_INJECTION_ENABLE Error Injection Enable 0 = Disable 1 = Enable
6:4	RW	0	R35 [6:4]: ERROR_INJECTION_RAIL_SELECTION Error Injection - Input Rail and Output Rail Selection 000 = Undefined 001 = SWA Output Only 010 = Reserved 011 = SWB Output Only 100 = SWC Output Only 101 = VIN_Bulk Input Only 110 = Reserved 111 = Do Not Use
3	RW	0	R35 [3]: OVER_VOLTAGE_UNDER_VOLTAGE_SELECT

R35 - Error Injection			
Bits	**Attribute**	**Default**	**Description**
			Over-Voltage or Under-Voltage Selection for Bits R35[6:4] 0 = Over-Voltage 1 = Under-Voltage
2:0	RW	0	R35 [2:0]: MISC_ERROR_INJECTION_TYPE Miscellaneous Error Injection Type 000 = Undefined 001 = Reserved 010 = Critical Temperature Shutdown 011 = High Temperature Warning Threshold 100= VOUT_1.8V LDO Power Good 101 = High Current Consumption Warning 110 = Reserved 111 = Current Limiter Warning

R36 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R36 [7:0]: Reserved

R37 - DIMM Vendor Region Password Lower Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	0111 0011	R37 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_LOWER_BYTE DIMM Vendor Memory Region (R40 - R6F) Password - Lower Byte [7:0] = Code

R38 - DIMM Vendor Region Password Upper Byte			
Bits	**Attribute**	**Default**	**Description**
7:0	WO	1001 0100	R38 [7:0]: DIMM_VENDOR_MEMORY_REGION_PASSWORD_UPPER_BYTE DIMM Vendor Memory Region (R40 - R6F) Password - Upper Byte [7:0] = Code

R39 - DIMM Vendor Password Control			
Bits	**Attribute**	**Default**	**Description**
7:0	RW	0	Host Region Codes: 0x74: Clear Registers R04 to R07, Erase MTP memory for R04 Register. DIMM Vendor Region (R40 to R6F) Write Codes: 0x00: Lock DIMM Vendor Region. 0x40: Unlock DIMM Vendor Region. Password needs to be present in R37 & R38 registers. 0x80: Burn DIMM Vendor Region Password. New password needs to be present in R37 & R38. 0x81: Burn DIMM Vendor Region - R40 to R4F

R39 - DIMM Vendor Password Control			
Bits	**Attribute**	**Default**	**Description**
			0x82: Burn DIMM Vendor Region - R50 to R5F 0x85: Burn DIMM Vendor Region - R60 to R6F DIMM Vendor Region (R40 to R6F) Read Codes: 0x5A: Burning is complete in DIMM Vendor region.

R3A – Default Address Pointer			
Bits	**Attribute**	**Default**	**Description**
7	RV	0	R3A [7]: Reserved
6	RW	0	R3A [6]: DEFAULT_READ_ADDRESS_POINTER_ENABLE Enable Default Address Read Pointer when PMIC sees STOP operation 0 = Disable Default Address Pointer (address pointer is set by Host) 1 = Enable Default Address Pointer; Address selected by register bits [5:4]
5:4	RW	0	R3A [5:4]: DEFAULT_READ_STARTING_ADDRESS Default Read Address Pointer Selection when PMIC sees STOP operation 00 = R08 01 = R0C 10 = Reserved 11 = Reserved
3:2	RW	0	R3A [3:2]: BURST_LENGTH_FOR_READ_DEFAULT_ADDR_POINTER Burst Length (# of Bytes) to be transferred for Read Default Address Pointer Mode 00 = 2 Bytes 01 = 4 Bytes 10 = Reserved 11 = 16 Bytes
1:0	RV	0	R3A [1:0]: Reserved

R3B - Revision ID, PMIC Current Capability Selection			
Bits	**Attribute**	**Default**	**Description**
7:6	RV	0	R3B [7:6]: Reserved
5:4	ROE	-	R3B [5:4]: REVISION_ID_MAJOR_STEPPING Major Revision Stepping 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	-	R3B [3:1]: REVISION_ID_MINOR_STEPPING Minor Revision Stepping 000 = Revision 0 001 = Revision 1 010 = Revision 2 011 = Revision 3

R3B - Revision ID, PMIC Current Capability Selection			
Bits	**Attribute**	**Default**	**Description**
			All other encodings are reserved.
0	RV	0	R3B [0]: Reserved

R3C - Vendor ID Byte0			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	1000 0110	R3C [7:0]: VENDOR_ID_BYTE0 Vendor Identification Register Byte 0.

R3D - Vendor ID Byte1			
Bits	**Attribute**	**Default**	**Description**
7:0	ROE	1100 1000	R3D [7:0]: VENDOR_ID_BYTE1 Vendor Identification Register Byte 1.

R3E - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R3E [7:0]: Reserved

R3F - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R3F [7:0]: Reserved

8.5.2 DIMM Vendor Region Registers

R40 - Power On Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R40 [7]: POWER_ON_SEQUENCE_CONFIG0 PMIC Power-On Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	0	R40 [6]: POWER_ON_SEQUENCE_CONFIG0_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R40 [5]: Reserved
4	RWPE	0	R40 [4]: POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	1	R40 [3]: POWER_ON_SEQUENCE_CONFIG0_SWC_ENABLE Enable Switch Node C Output Regulator.

R40 - Power On Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
			0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R40 [2:0]: POWER_ON_SEQUENCE_CONFIG0_IDLE Idle time after Power-On Sequence Config0 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

(Note: The R40[4] POWER_ON_SEQUENCE_CONFIG0_SWB_ENABLE setting need to be the same as SWA R40[6] in dual phase mode operation.)

R41 - Power-On Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R41 [7]: POWER_ON_SEQUENCE_CONFIG1 PMIC Power-On Sequence Config 1 0 = Do Not Execute Config 1 = Execute Command 1
6	RWPE	1	R41 [6]: POWER_ON_SEQUENCE_CONFIG1_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R41 [5]: Reserved
4	RWPE	1	R41 [4]: POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	1	R41 [3]: POWER_ON_SEQUENCE_CONFIG1_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	001	R41 [2:0]: POWER_ON_SEQUENCE_CONFIG1_IDLE Idle time after Power-On Sequence Config1 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms

R41 - Power-On Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
			101 = 10ms 110 = 12ms 111 = 24ms

(Note: The R41[4] POWER_ON_SEQUENCE_CONFIG1_SWB_ENABLE setting need to be the same as SWA R41[6] in dual phase mode operation.)

R42 - Power-On Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R42 [7]: POWER_ON_SEQUENCE_CONFIG2 PMIC Power-On Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	R42 [6]: POWER_ON_SEQUENCE_CONFIG2_SWA_ENABLE Enable Switch Node A Output Regulator. 0 = Disable Switch Node A Output Regulator 1 = Enable Switch Node A Output Regulator
5	RV	0	R42 [5]: Reserved
4	RWPE	0	R42 [4]: POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE Enable Switch Node B Output Regulator. 0 = Disable Switch Node B Output Regulator 1 = Enable Switch Node B Output Regulator
3	RWPE	0	R42 [3]: POWER_ON_SEQUENCE_CONFIG2_SWC_ENABLE Enable Switch Node C Output Regulator. 0 = Disable Switch Node C Output Regulator 1 = Enable Switch Node C Output Regulator
2:0	RWPE	000	R42 [2:0]: POWER_ON_SEQUENCE_CONFIG2_IDLE Idle time after Power-On Sequence Config2 000 = 0ms 001 = 2ms 010 = 4ms 011 = 6ms 100 = 8ms 101 = 10ms 110 = 12ms 111 = 24ms

(Note: The R42[4] POWER_ON_SEQUENCE_CONFIG2_SWB_ENABLE setting need to be the same as SWA R42[6] in dual phase mode operation.)

R43 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R43 [7:0]: Reserved

R44 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R44 [7:0]: Reserved

R45 - SWA Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R45 [7:1]: SWA_VOLTAGE_SETTING Switch Node A Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV … 011 1100 = 1100mV … 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RWPE	0	R45 [0]: SWA_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold Low-Side Voltage For Power Good Status 0 = -5% from the setting in “Register R45” [7:1] 1 = -7.5% from the setting in “Register R45” [7:1]

R46 - SWA Threshold and Soft stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R46 [7:6]: SWA_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node A Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R45” [7:1] 01 = +7.5% from the setting in “Register R45” [7:1] 10 = +10% from the setting in “Register R45” [7:1] 11 = +3% from the setting in “Register R45” [7:1]
5:4	RWPE	10	R46 [5:4]: SWA_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R45” [7:1] 01 = +10% from the setting in “Register R45” [7:1] 10 = +12.5% from the setting in “Register R45” [7:1] 11 = +20% from the setting in “Register R45” [7:1]
3:2	RWPE	00	R46 [3:2]: SWA_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node A Output Regulator Threshold For Under-Voltage Lockout Status 00 = -10% from the setting in “Register R45” [7:1] 01 = -12.5% from the setting in “Register R45” [7:1]

R46 - SWA Threshold and Soft stop Time			
Bits	**Attribute**	**Default**	**Description**
			10 = -7.5% from the setting in “Register R45” [7:1] 11 = -20% from the setting in “Register R45” [7:1]
1:0	RWPE	11	R46 [1:0]: SWA_OUTPUT_SOFT_STOP_TIME SWA Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R47- Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R47 [7:0]: Reserved

R48 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R48 [7:0]: Reserved

R49 - SWB Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R49 [7:1]: SWB_VOLTAGE_SETTING Switch Node B Output Regulator Voltage Setting 000 0000 = 800mV 000 0001 = 805mV 000 0010 = 810mV … 011 1100 = 1100mV … 111 1101 = 1425mV 111 1110 = 1430mV 111 1111 = 1435mV
0	RWPE	0	R49 [0]: SWB_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold Low-Side Voltage For Power Good Status 0 = -5% from the setting in “Register R49” [7:1] 1 = -7.5% from the setting in “Register R49” [7:1]

R4A - SWB Threshold and Soft stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4A [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node B Output Threshold High-Side Voltage “Upper bound” For Power Good Status

R4A - SWB Threshold and Soft stop Time			
Bits	**Attribute**	**Default**	**Description**
			00 = +5% from the setting in “Register R49” [7:1] 01 = +7.5% from the setting in “Register R49” [7:1] 10 = +10% from the setting in “Register R49” [7:1] 11 = +3% from the setting in “Register R49” [7:1]
5:4	RWPE	10	R4A [5:4]: SWB_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over-Voltage Status 00 = +7.5% from the setting in “Register R49” [7:2] 01 = +10% from the setting in “Register R49” [7:1] 10 = +12.5% from the setting in “Register R49” [7:1] 11 = +20% from the setting in “Register R49” [7:1]
3:2	RWPE	00	R4A [3:2]: SWB_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under-Voltage Lockout Status 00 = -10% from the setting in “Register R49” [7:1] 01 = -12.5% from the setting in “Register R49” [7:1] 10 = -7.5% from the setting in “Register R49” [7:1] 11 = -20% from the setting in “Register R49” [7:1]
1:0	RWPE	11	R4A [1:0]: SWB_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 0.5ms 01 = 1ms 10 = 2ms 11 = 4ms

R4B - SWC Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:1	RWPE	0111100	R4B [7:1]: SWC_VOLTAGE_SETTING Switch Node C Output Regulator Voltage Setting2 000 0000 = 1500mV 000 0001 = 1505mV 000 0010 = 1510mV … 011 1100 = 1800mV … 111 1101 = 2125mV 111 1110 = 2130mV 111 1111 = 2135mV
0	RWPE	0	R4B [0]: SWC_POWER_GOOD_THRESHOLD_LOW_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold Low-Side Voltage For Power Good Status 0 = -5% from the setting in “Register R4B” [7:1] 1 = -7.5% from the setting in “Register R4B” [7:1]

R4C - SWC Threshold and Soft stop Time			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R4C [7:6]: SWC_POWER_GOOD_THRESHOLD_HIGH_SIDE_VOLTAGE_SETTING Switch Node C Output Threshold High-Side Voltage “Upper bound” For Power Good Status 00 = +5% from the setting in “Register R4B” [7:1] 01 = +7.5% from the setting in “Register R4B” [7:1] 10 = +10% from the setting in “Register R4B” [7:1] 11 = +3% from the setting in “Register R4B” [7:1]
5:4	RWPE	10	R4C [5:4]: SWC_OVER_VOLTAGE_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Over-Voltage Status 00 =+7.5% from the setting in “Register R4B” [7:1] 01 = +10% from the setting in “Register R4B” [7:1] 10 = +12.5% from the setting in “Register R4B” [7:1] 11 = +20% from the setting in “Register R4B” [7:1]
3:2	RWPE	00	R4C [3:2]: SWC_UNDER_VOLTAGE_LOCKOUT_THRESHOLD_SETTING Switch Node C Output Regulator Threshold For Under-Voltage Lockout Status 00 = -10% from the setting in “Register R4B” [7:1] 01 = -12.5% from the setting in “Register R4B” [7:1] 10 = -7.5% from the setting in “Register R4B” [7:1] 11 = -20% from the setting in “Register R4B” [7:1]
1:0	RWPE	11	R4C [1:0]: SWC_OUTPUT_SOFT_STOP_TIME SWC Output Regulator Soft-Stop Time After VR Disable 00 = 1ms 01 = 2ms 10 = 4ms 11 = 8ms

R4D - SWA FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4D [7:6]: SWA_MODE_SELECT Switch Node A Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4D [5:4]: SWA_SWITCHING_FREQ Switch Node A Output Regulator Switching Frequency (Note) 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

R4D - SWA FSW & Mode			
Bits	**Attribute**	**Default**	**Description**
3:0	RV	0000	R4D [3:0]: Reserved

R4E - SWB, SWC FSW & Mod			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	10	R4E [7:6]: SWB_MODE_SELECT Switch Node B Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
5:4	RWPE	00	R4E [5:4]: SWB_SWITCHING_FREQ Switch Node B Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz
3:2	RWPE	10	R4E [3:2]: SWC_MODE_SELECT Switch Node D Output Regulator Mode Selection 00 = Reserved 01 = Reserved 10 = COT; DCM (Constant on Time; Discontinuous Current Mode) 11 = COT; Forced CCM (Constant on Time; Continuous Current Mode)
1:0	RWPE	00	R4E [1:0]: SWC_SWITCHING_FREQ Switch Node C Output Regulator Switching Frequency 00 = 750kHz 01 = 1000kHz 10 = 1250kHz 11 = 1500kHz

R4F - Phase Mode Select			
Bits	**Attribute**	**Default**	**Description**
7:1	RV	0	R4F [7:1]: Reserved
0	RWPE	0	R4F [0]: SWA_SWB_PHASE_MODE_SELECT Switch Node A and Switch Node B Phase Regulator Mode Selection. 0 = Single Phase Regulator Mode 1 = Dual Phase Regulator Mode

R50 - Output Current Limit			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	00	R50 [7:6]: SWA_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node A Output Current Limiter Warning Threshold Setting

R50 - Output Current Limit			
Bits	**Attribute**	**Default**	**Description**
			For COT Mode, Ivalley_limit: 00 = 5.0A 01 = 5.5A 10 = 6.0A 11 = Reserved
5:4	RV	00	R50 [5:4]: Reserved
3:2	RWPE	00	R50 [3:2]: SWB_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node B Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 5.0A 01 = 5.5A 10 = 6.0A 11 = Reserved
1:0	RWPE	11	R50 [1:0]: SWC_OUTPUT_CURRENT_LIMITER_WARNING_THRESHOLD_SETTING Switch Node C Output Current Limiter Warning Threshold Setting For COT Mode, Ivalley_limit: 00 = 0.5A 01 = 1.0A 10 = 1.5A 11 = 2.0A

R51 - LDO Voltage Setting			
Bits	**Attribute**	**Default**	**Description**
7:6	RWPE	01	R51 [7:6]: VOUT_1.8V _VOLTAGE_SETTING VLDO_1.8V Voltage Setting: 00 = 1.7V 01 = 1.8V 10 = 1.9V 11 = 2.0V
5:3	RV	000	R51 [5:3]: Reserved
2:1	RWPE	01	R51 [2:1]: VOUT_1.0V _VOLTAGE_SETTING VLDO_1.0V Voltage Setting: 00 = 0.9V 01 = 1.0V 10 = 1.1V 11 = 1.2V
0	RV	0	R51 [0]: Reserved

R52-R57 - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R52 [7:0] - R57 [7:0]: Reserved

R58 - Power Off Sequence Configuration 0			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R58 [7]: POWER_OFF_SEQUENCE_CONFIG0 PMIC Power Off Sequence Config0 0 = Do Not Execute Config0 1 = Execute Config0
6	RWPE	1	R58 [6]: POWER_OFF_SEQUENCE_CONFIG0_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R58 [5]: Reserved
4	RWPE	1	R58 [4]: POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE Enable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R58 [3]: POWER_OFF_SEQUENCE_CONFIG0_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	R58 [2:0]: POWER_OFF_SEQUENCE_CONFIG0_IDLE Idle time after Power Off Sequence Config0 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

(Note: The R58[4] POWER_OFF_SEQUENCE_CONFIG0_SWB_DISABLE setting need to be the same as SWA R58[6] in dual phase mode operation.)

R59 - Power Off Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	1	R59 [7]: POWER_OFF_SEQUENCE_CONFIG1 PMIC Power Off Sequence Config1 0 = Do Not Execute Config1 1 = Execute Config1
6	RWPE	1	R59 [6]: POWER_OFF_SEQUENCE_CONFIG1_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator

R59 - Power Off Sequence Configuration 1			
Bits	**Attribute**	**Default**	**Description**
5	RV	0	R59 [5]: Reserved
4	RWPE	1	R59 [4]: POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE Enable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	1	R59 [3]: POWER_OFF_SEQUENCE_CONFIG1_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator
2:0	RWPE	001	R59 [2:0]: POWER_OFF_SEQUENCE_CONFIG1_IDLE Idle time after Power Off Sequence Config1 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

(Note: The R59[4] POWER_OFF_SEQUENCE_CONFIG1_SWB_DISABLE setting need to be the same as SWA R59[6] in dual phase mode operation.)

R5A - Power Off Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
7	RWPE	0	R5A [7]: POWER_OFF_SEQUENCE_CONFIG2 PMIC Power Off Sequence Config2 0 = Do Not Execute Config2 1 = Execute Config2
6	RWPE	0	R5A [6]: POWER_OFF_SEQUENCE_CONFIG2_SWA_DISABLE Disable Switch Node A Output Regulator. 0 = Do Not Disable Switch Node A Output Regulator 1 = Disable Switch Node A Output Regulator
5	RV	0	R5A [5]: Reserved
4	RWPE	0	R5A [4]: POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE Enable Switch Node B Output Regulator. 0 = Do Not Disable Switch Node B Output Regulator 1 = Disable Switch Node B Output Regulator
3	RWPE	0	R5A [3]: POWER_OFF_SEQUENCE_CONFIG2_SWC_DISABLE Disable Switch Node C Output Regulator. 0 = Do Not Disable Switch Node C Output Regulator 1 = Disable Switch Node C Output Regulator

R5A - Power Off Sequence Configuration 2			
Bits	**Attribute**	**Default**	**Description**
2:0	RWPE	000	R5A [2:0]: POWER_OFF_SEQUENCE_CONFIG2_IDLE Idle time after Power Off Sequence Config2 000 = 0ms 001 = 1ms 010 = 2ms 011 = 3ms 100 = 4ms 101 = 5ms 110 = 6ms 111 = 7ms

(Note: The R5A[4] POWER_OFF_SEQUENCE_CONFIG2_SWB_DISABLE setting need to be the same as SWA R5A[6] in dual phase mode operation.)

R5B - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5B [7:0]: Reserved

R5C - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5C [7:0]: Reserved

R5D - SWA Soft Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5D [7:5]: SWA_OUTPUT_SOFT_START_TIME SWA Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
4:0	RV	0	R5D [4:0]: Reserved

R5E - SWB, SWC Soft Start Time			
Bits	**Attribute**	**Default**	**Description**
7:5	RWPE	001	R5E [7:5]: SWB_OUTPUT_SOFT_START_TIME SWB Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms

R5E - SWB, SWC Soft Start Time			
Bits	**Attribute**	**Default**	**Description**
			... 111 = 14ms
4	RV	0	R5E [4]: Reserved
3:1	RWPE	001	R5E [3:1]: SWC_OUTPUT_SOFT_START_TIME SWC Output Regulator Soft-Start Time After VR Enable 000 = 1ms 001 = 2ms 010 = 4ms 011 = 6ms ... 111 = 14ms
0	RV	0	R5E [0]: Reserved

R5F-R6F - Reserved			
Bits	**Attribute**	**Default**	**Description**
7:0	RV	0	R5F [7:0] – R6F [7:0]: Reserved

9 Layout Guidelines and Example

Layout is very important in high frequency switching converter design. If designed improperly, the PCB could radiate excessive noise and contribute to the converter instability. Certain points must be considered before starting a layout for GD30MP1020. Figure 11, show the recommended layout guide for reference. In Figure 11, the top layer layout of GD30MP1020's EVB is demonstrated. It should be noticed that the components' size is considered and drawn in real relating size. Four inductors and one PMIC are on the same layer to avoid the necessary of phase node vias which can induce large phase ringing and EMI noise. Two bulk capacitors are placed at the same side the VIN pin for each rail. Place the small decoupling capacitor can help to filter out the high frequency voltage spike, reduce the phase ringing on phase pin. Bulk capacitors can provide prompt energy during output load transient. Most important thing is to keep away the noisy signal, like switching node, output caps' vias. Below are the key items of GD30MP1020's EVB layout.

- Make traces of the high current paths as short and wide as possible.
- Put the input capacitor as close as possible to the device pins (VINA, VINB and VINC).
- The SW node encounters high frequency voltage swings so it should be kept in a small area. Keep sensitive components away from the SW node to prevent noise couple.
- The PGND pin should be connected to a strong ground plane for heat sinking and noise protection. For better power dissipation, adding thermal vias near PGND pin to connect between different layers is recommended.
- The ground of VIN is recommended to connect to AGND then connect to PGND layer through via.
- Place the decoupling capacitors as close as possible to the device pins (VIN and AGND).
- Differential routing the feedback traces for each rail and keep away from noisy signal on the EVB.
- The NC pins at the four corners are recommended to connect to PGND for better heat dissipation.
- For the dual-phase application, must put the output capacitors (COUTA and COUTB) as close as possible, and put the sense feedback node of SWA_FB_P at the center of VDD and VDDQ is needed.

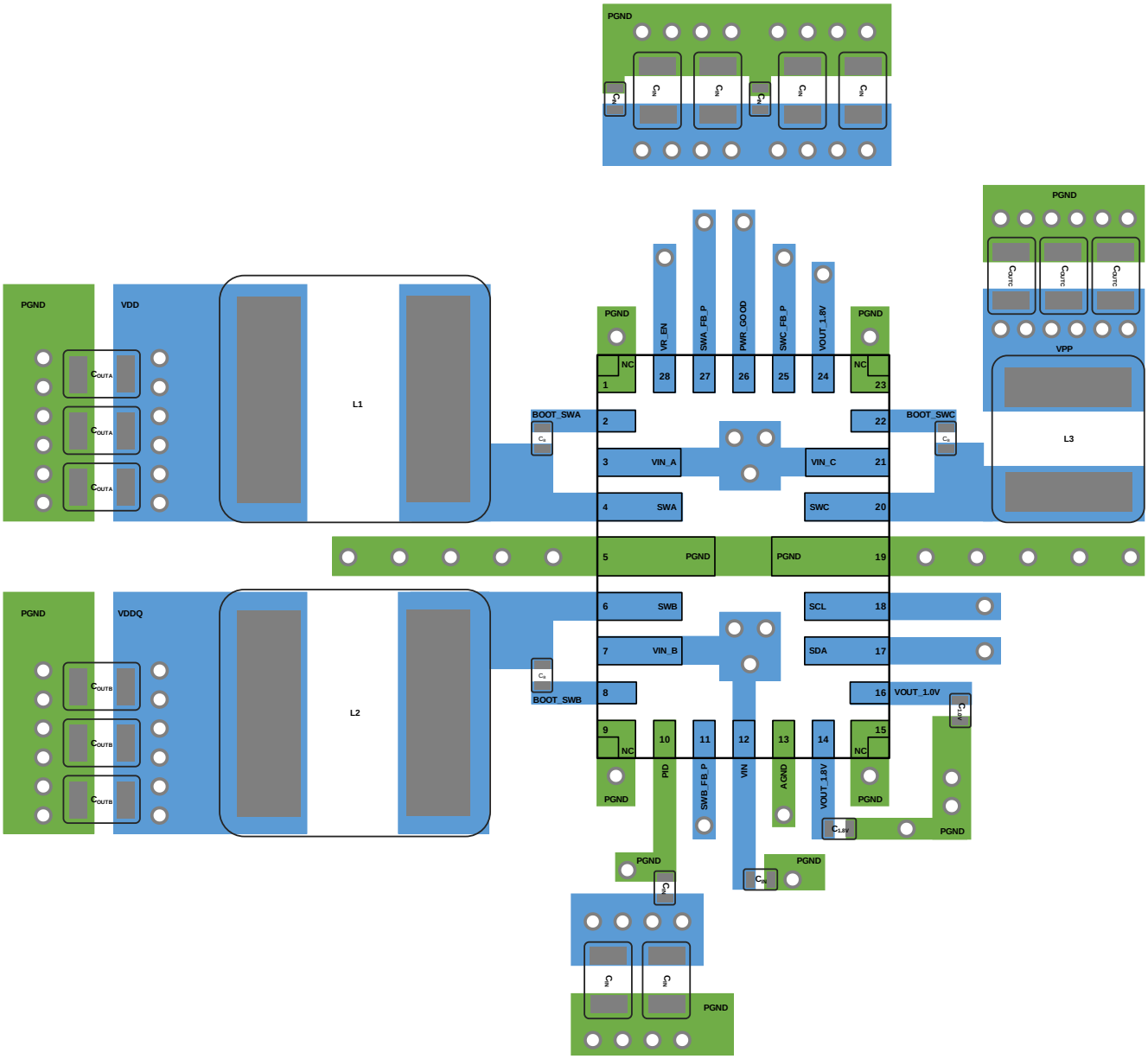
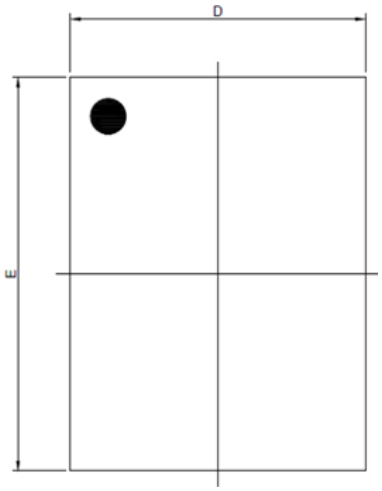


Figure 11. Typical GD30MP1020 Example Layout

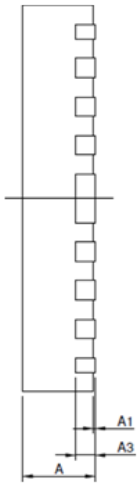
10 Package Information

10.1 Outline Dimensions

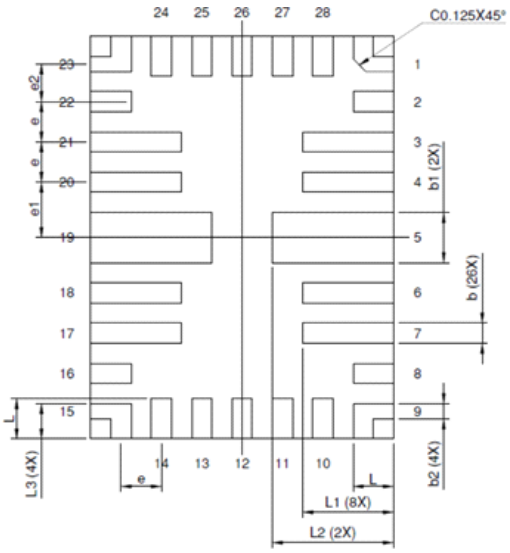
WQFN-28L Package Outline



TOP VIEW



SIDE VIEW



BOTTOM VIEW

NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 11. *WQFN-28L Dimensions(mm)*.

Table 11. WQFN-28L Dimensions(mm)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
b1	0.45	0.50	0.55
b2	0.10	0.15	0.20
D	2.95	3.00	3.05
E	3.95	4.00	4.05
e		0.40 BSC	
e1		0.55 BSC	
e2		0.375 BSC	
L	0.35	0.40	0.45
L1	0.85	0.90	0.95
L2	1.15	1.2	1.25
L3	0.30	0.35	0.40

11 Ordering information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30MP1020GUTR-I	WQFN-28L	Green	Tape & Reel	3000	−10°C to +125°C

12 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2024
1.1	Modiy SWA、SWB、SWC Current Limit	2024

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