Over-Voltage and Over-Current Protection IC

1 Features

- Robust Protection
  - Input Over-Voltage Protection
  - Input Over-Current Protection
  - Output Short-Circuit Protection
  - Thermal Shutdown
- Soft-Start to Prevent Inrush Current
- Soft-Stop to Prevent Voltage Spikes
- Maximum Input Voltage of 30V
- Fixed OVLO Threshold Voltage: 6.0V
- Over Current Protection Threshold: 1.5A
- OVP Response time: 450ns
- 100μA Low Quiescent Current
- Low $R_{DS(ON)}$ Integrated MOSFET: 85mΩ
- Small 2mm x 2mm 8pin DFN Package
- RoHS Compliant and Halogen Free

2 Applications

- True Wireless Stereo(TWS)
- Portables and Mobile Device
- Smart Phones
- Low Voltage Peripherals

3 Description

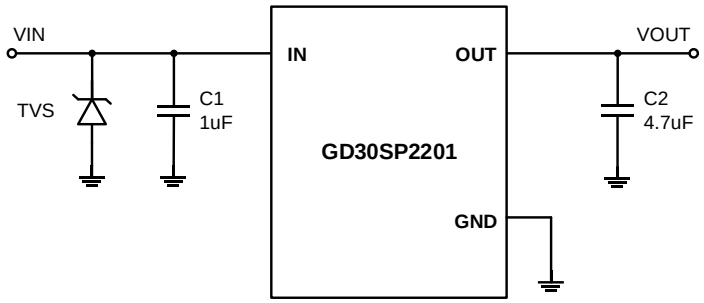
The GD30SP2201 is a highly integrated circuit designed to provide protection to low voltage system from failures of the high input voltage. The device continuously monitors the input voltage, and the input current. When the input overvoltage condition is occur, the device will turn off the power MOSFET immediately. If the input current exceeds the over current threshold for a limited time, the device will turn off the output power. Additionally, the device also provide other protection features include under voltage lockout and thermal shutdown. The GD30SP2201 is available in a green small foot print DFN2×2-8L package.

Device Information[1]

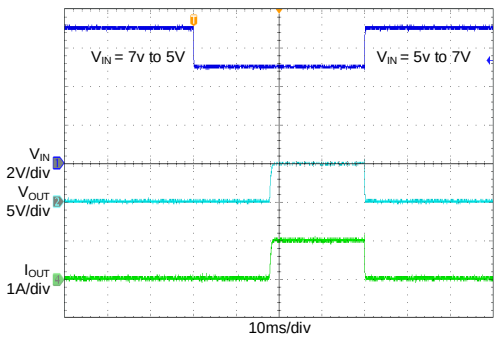
PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30SP2201	DFN8L	2.00mm x 2.00mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic



OVP Entry and Recovery



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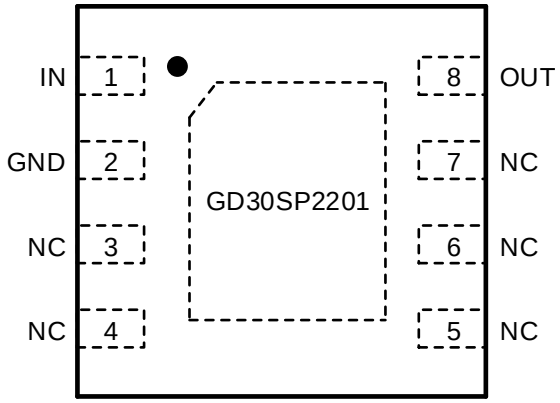
4 Device Overview

4.1 Pinout and Pin Assignment

DFN Package
8pin DFN With Exposed Thermal Pad
Top View



4.2 Pin Description

PIN NUMBER		PIN TYPE[1]	FUNCTION
NAME	NUM		
IN	1	I	Power Supply Voltage Input. A general 1μF ceramic capacitor should be placed as close as possible to this pin.
GND	2	G	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
NC	3,4,5,6,7		No connection pin for GD30SP2201.
OUT	8	O	Output of the Regulator. A general 4.7μF ceramic capacitor should be placed as close as possible to this pin.
Thermal PAD		G	The thermal pad must be connected to ground.

1. I = Input, O = Output, G = Ground.

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5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range(unless otherwise noted)[1]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{IN}	Input voltage(with respect to GND)	−0.3	30	V
V_{OUT}	Output voltage(with respect to GND)	−0.3	7	V
I_{IN}	Output current		1.5	A
T_J	Operating junction temperature	−40	150	°C
T_{stg}	Storage temperature	−65	150	°C
P_{max}	Maximum power dissipation @ T_A=+25°C		0.5	W

1. The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

5.2 Recommended Operation Conditions

SYMBOL[1,2]	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	2.5		30	V
I_{IN}	Input current			1.2	A
I_{OUT}	Output current			1.2	A
T_J	Operating junction temperature	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Refer to the *Application Information* section for further information.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±500	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	PACKAGE	VALUE	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	DFN8L	86.45	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	DFN8L	36.25	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	DFN8L	47.13	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	DFN8L	36.20	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	DFN8L	3.61	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{IN} = 5V, T_J = 25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
IN						
V_{UVLO}	Under voltage lockout	V_{IN} rising		2.25	2.45	V
V_{UVLO_HYS}	Under voltage lockout hysteresis			250		mV
I_Q	Quiescent current	No load on OUT pin		110		μA
t_{BLK}	Input power on blanking time	VIN rising to VOUT rising		18		ms
INPUT TO OUT CHARACTERISTICS						
$R_{DS(on)}$	On resistance form IN to OUT	I_{OUT} = 1.0A		85		mΩ
INPUT OVERVOLTAGE PROTECTION						
V_{OVP}	Input overvoltage protection threshold	VIN rising		6		V
t_{OVP}	Input overvoltage protection response time			450		ns
$t_{REC(OVP)}$	Input OVP recovery time			18		ms
INPUT OVERCURRENT PROTECTION						
I_{OCP}	OCP threshold		1.5			A
t_{DGL}	Input OCP deglitch time			3		ms
$t_{REC(OVP)}$	Input OCP recovery time			18		ms
THERMAL SHUTDOWM						
T_{TSD}	Thermal shutdown temperature[1]			150		°C
T_{HYS}	Thermal shutdown hysteresis[1]			20		°C

1. Guaranteed by design and engineering sample characterization.

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5.6 Typical Characteristics

V_{IN} = 5V, C_{IN} = 1μF, C_{OUT} = 4.7μF, unless otherwise noted.

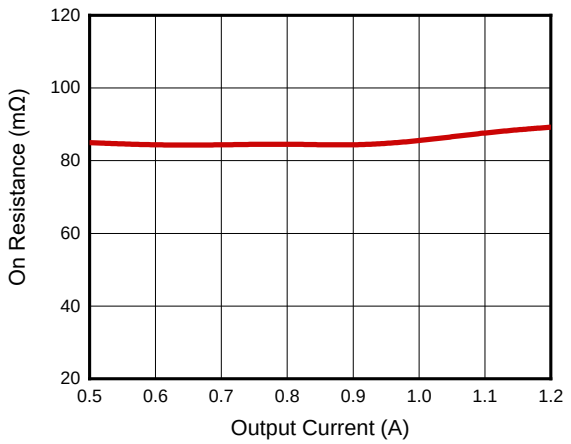

Figure 1. On Resistance vs. Output Current

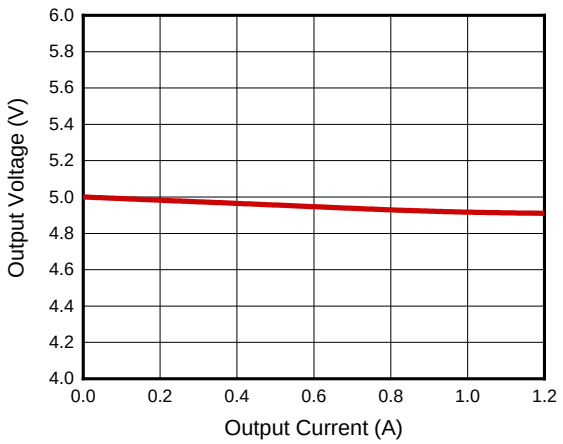

Figure 2. Output Voltage vs. Output Current

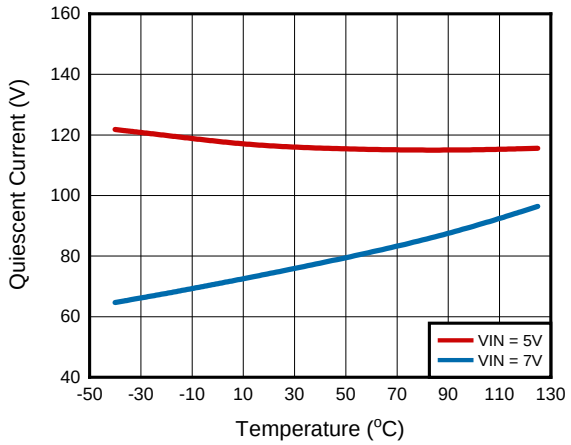

Figure 3. Quiescent Current vs. Temperature

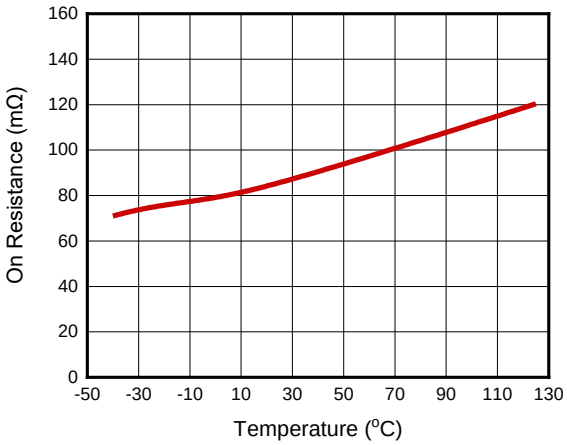

Figure 4. On Resistance vs. Temperature

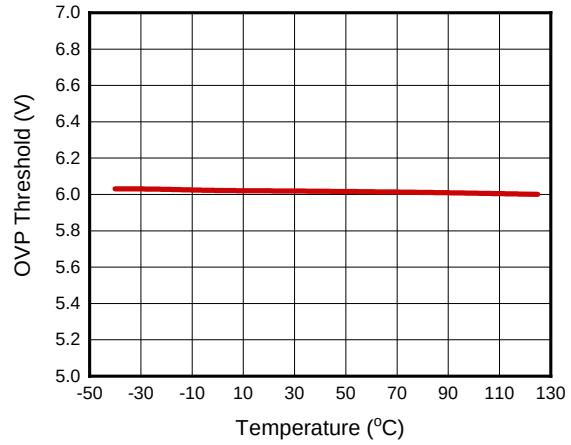

Figure 5. OVP Threshold vs. Temperature

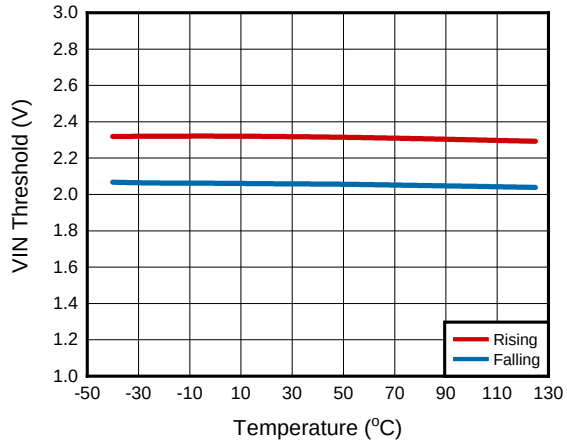

Figure 6. VIN UVLO Threshold vs. Temperature

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6 Functional Description

6.1 Block Diagram

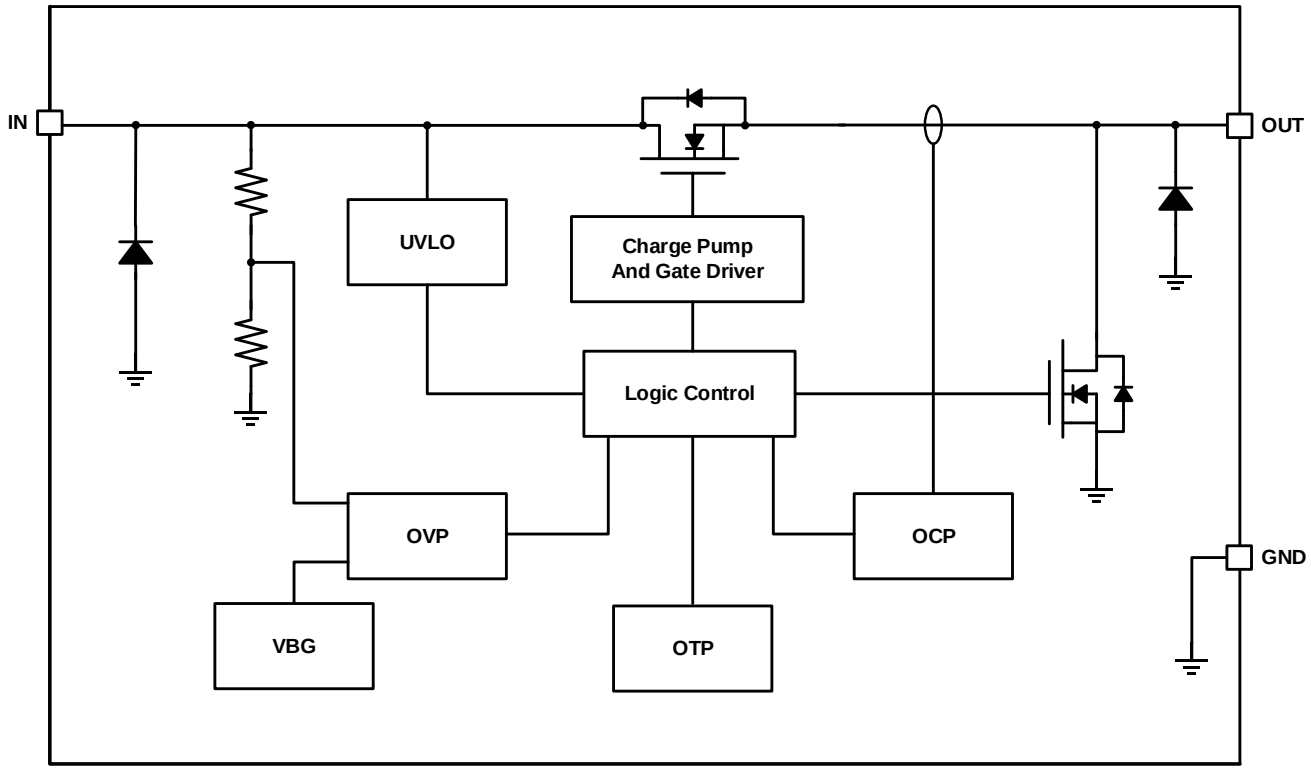

Figure 7. GD30SP2201 Functional Block Diagram

6.2 Operation

The GD30SP2201 is a highly integrated circuit designed to provide protection to low voltage system from failures of the high input voltage. The device continuously monitors the input voltage, and the input current. When the input overvoltage condition is occur, the device will turn off the power MOSFET after a blanking time. If the input current exceeds the over current threshold for a limited time, the device will turn off the output power. Additionally, the device also provide other protection features include under voltage lockout and thermal shutdown.

6.2.1 Input Overvoltage Protection

The GD30SP2201 has input over-voltage protection to prevent high voltage on IN passing through to OUT. Once the voltage on input exceeds the OVP threshold 6V(typical), the power MOSFET will be turned off immediately, 450ns(typical). When VIN drop back below OVP release level, the power MOSFET will be turned on again after a 18ms recovery time. Figure 8 shows the typical input OVP performance.

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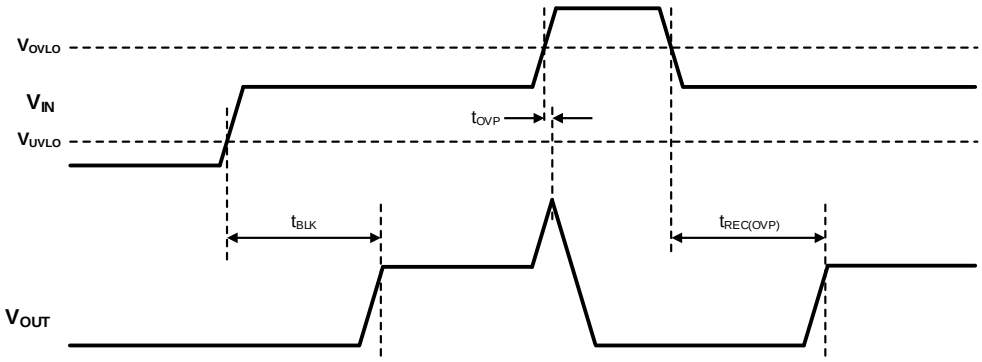

Figure 8. Input OVP Timing Diagram

6.2.2 Input Overcurrent Protection

The OCP feature ensures that the device will turn off power MOSFET when current through the switch exceed OCP threshold, I_{OCP}. If the input current through the device attempts to exceed the OCP threshold, the power MOSFET is opened only enough to maintain the current at the OCP level. If the current limiting condition is maintained longer than the deglitch time, t_{DGL}, the power MOSFET is closed completely in OCP recovery time, $t_{REC(OCP)}$, as shown in Figure 9. If the load current through the device attempts to exceed the OCP threshold, the hiccup behavior will continue as long as the heavy loading condition exist.

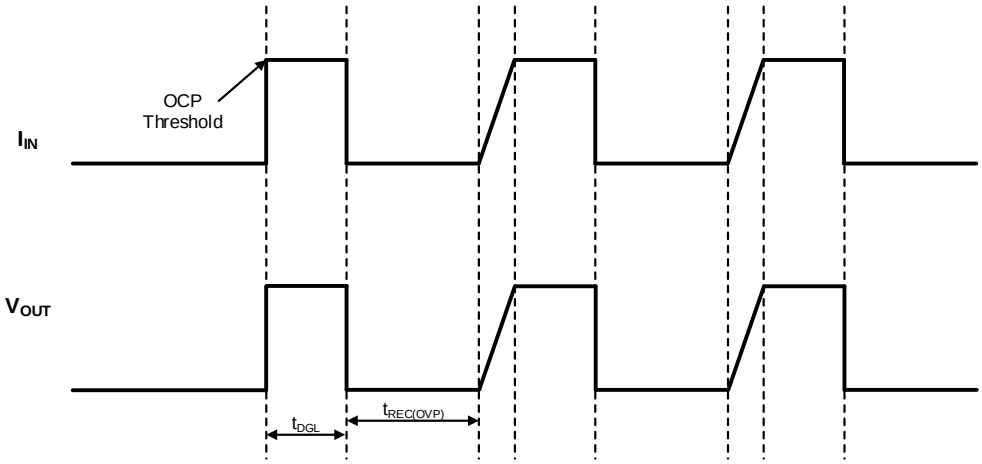

Figure 9. Input OCP Timing Diagram

6.2.3 Under Voltage Lockout

To avoid mis-operation of the device at an insufficient supply voltage, implement under voltage locking to shutdown the device when the voltage is below the V_{HYS} hysteresis of the V_{UVLO}.

6.2.4 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to turn off power MOSFET if the junction temperature exceeds 150°C(typical). Once the device temperature falls below the threshold with hysteresis 20°C (typical), the device returns to normal operation automatically.

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7 Application Information

The GD30SP2201 device provide overvoltage and overcurrent protection to low voltage system from faulty adapter or other input sources. If any of these faults occur, the GD30SP2201 device isolates the downstream devices from the input source.

7.1 Typical Application Circuit

The typical values for an application are V_{OVP} = 6V, I_{OCP} = 1.5A.

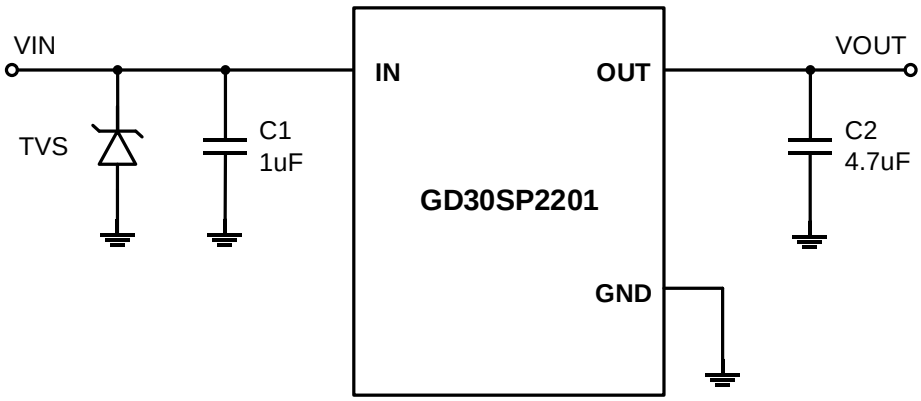

Figure 10. Typical Application Circuit

7.2 Design Example

For this design example, use the parameters in Table 1.

Table 1. Design Parameters

PARAMETER	EXAMPLE VALUE
Supply Voltage	5 V
Output Current	1 A

Table 2 lists the components used for the example.

Table 2. Design Example Component[1,2]

COMPONENT	DESCRIPTION
C1	1μF, Ceramic Capacitor, 25V, X7R, size 0603
C2	4.7μF, Ceramic Capacitor, 25V, X7R, size 0603
TVS	Surge protection, select according to actual application conditions

1. The components used in these design cases do not belong to GD products, GD does not warrant its accuracy or completeness. GD's customers need to test and verify whether the selected components meet their intended use to ensure stable system operation.
2. Refer to *Detailed Design Description* section for guidance on component selection.

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7.3 Detailed Design Description

7.3.1 Input and Output Bypass Capacitors Selection

The input capacitor C1 is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. C1 prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1μF be used at the input of the device. It should be located in close proximity to the input pin.

C2 should also be a ceramic capacitor of at least 4.7μF, located closed to the output pin. C2 also serves as the input decoupling capacitor for the subsequent circuit downstream of the protection IC.

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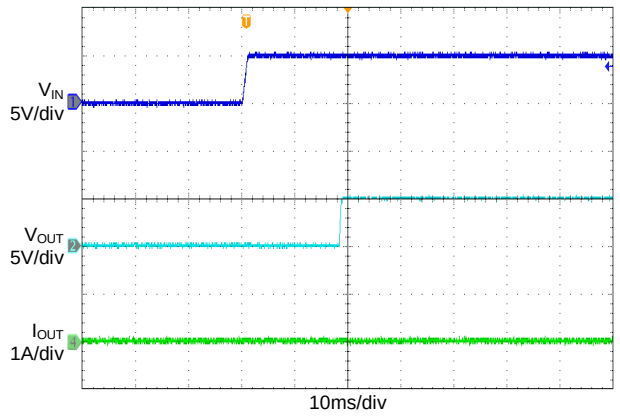
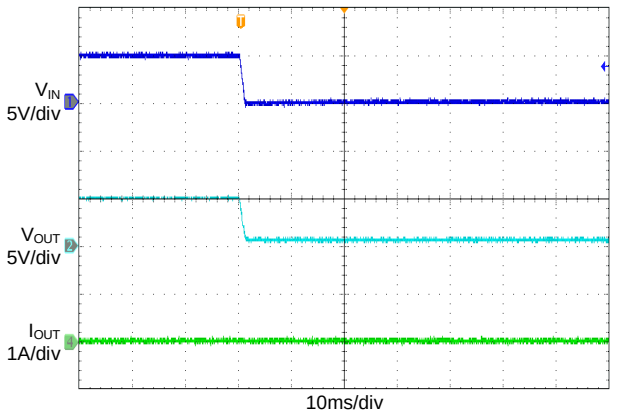
7.4 Typical Application Curves

V_{IN} = 5V, C_{IN} = 1μF, C_{OUT} = 4.7μF, T_A = 25°C, unless otherwise noted.



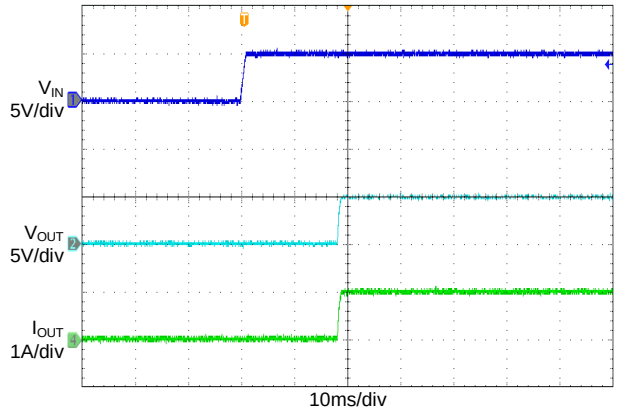
I_{OUT} = 0A

Figure 11. Power ON without Load



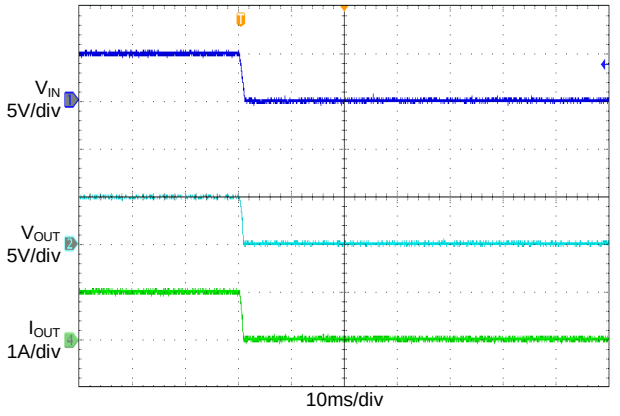
I_{OUT} = 0A

Figure 12. Power OFF without Load



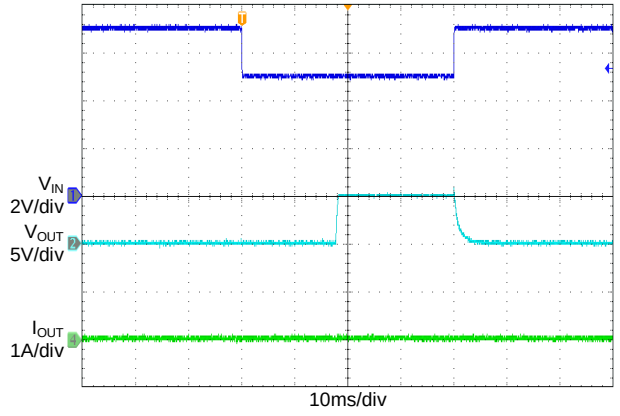
I_{OUT} = 1.0A

Figure 13. Power ON with Load



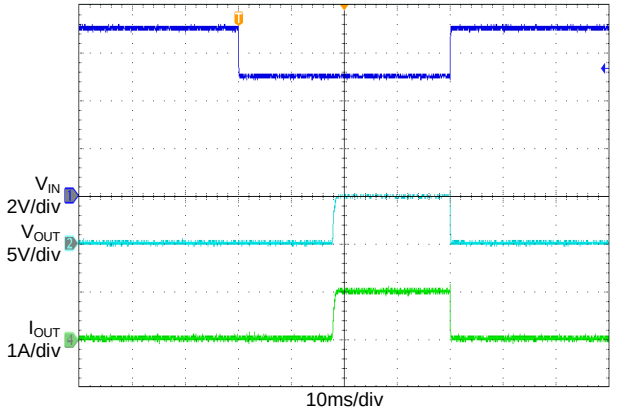
I_{OUT} = 1.0A

Figure 14. Power OFF with Load



V_{IN} = 7V to 5V to 7V, I_{OUT} = 0A

Figure 15. OVP Entry and Recovery without Load



V_{IN} = 7V to 5V to 7V, I_{OUT} = 1.0A

Figure 16. OVP Entry and Recovery with Load

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Typical Application Curves (continued)

V_{IN} = 5V, C_{IN} = 1μF, C_{OUT} = 4.7μF, T_A = 25°C, unless otherwise noted.

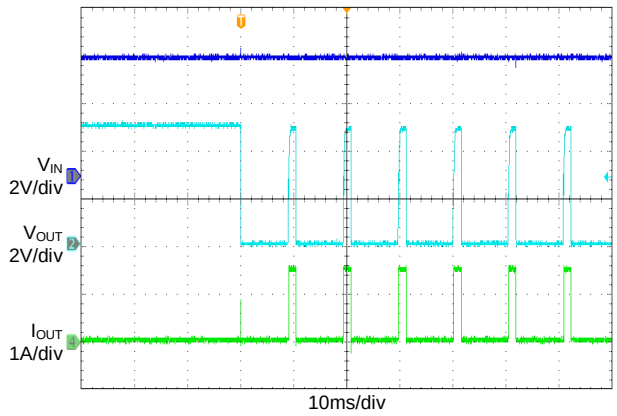

Figure 17. OCP Entry

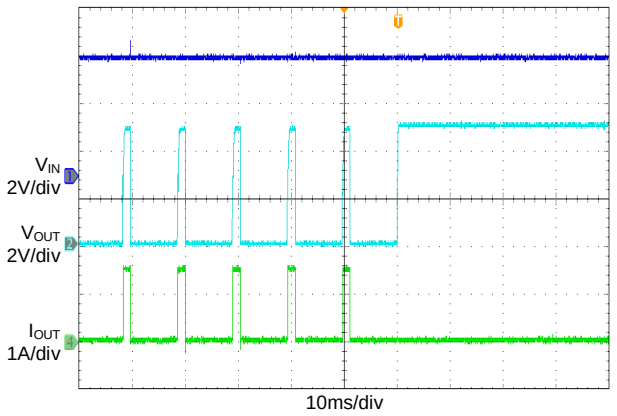

Figure 18. OCP Recovery

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8 Layout Guidelines and Example

Efficient PCB layout is critical for stable operation. To make fully use of the performance of GD30SP2201, the guidelines below should be followed.

1) Place the input/output capacitor and inductor should be placed as close to IC.
2) Keep the power traces as short as possible.
3) The device uses DFN package with a ThermalPAD™ . For good thermal performance, the ThermalPAD™ should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the device. This copper pad should be connected to the ground plane with an array of thermal vias.

For best results, follow the layout example below.

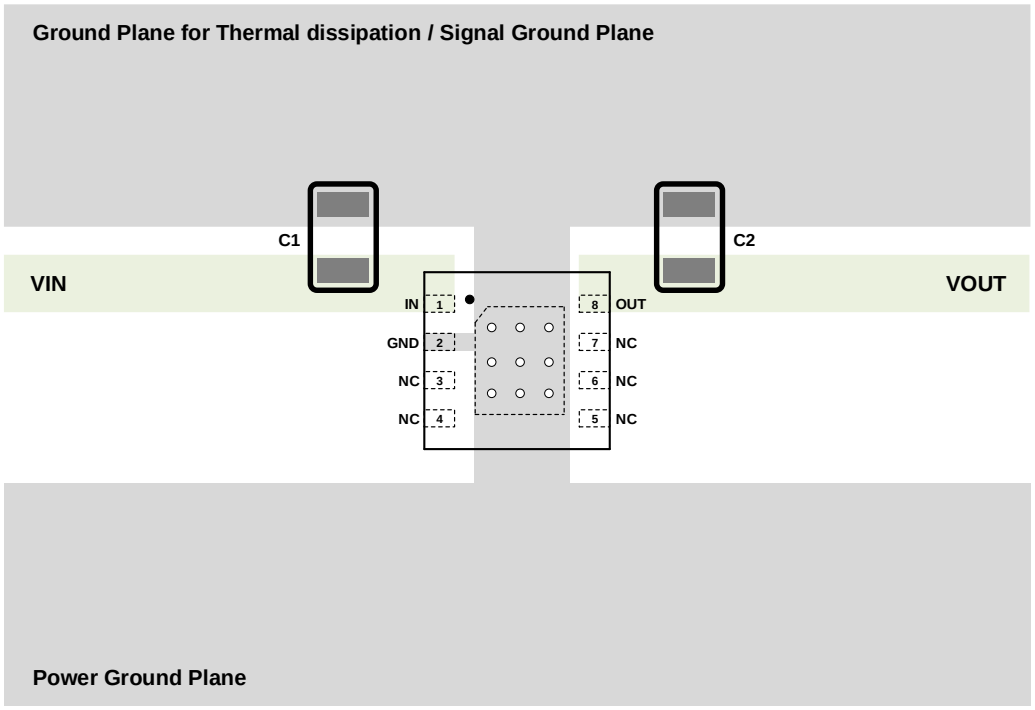

Figure 19. Typical GD30SP2201 Example Layout

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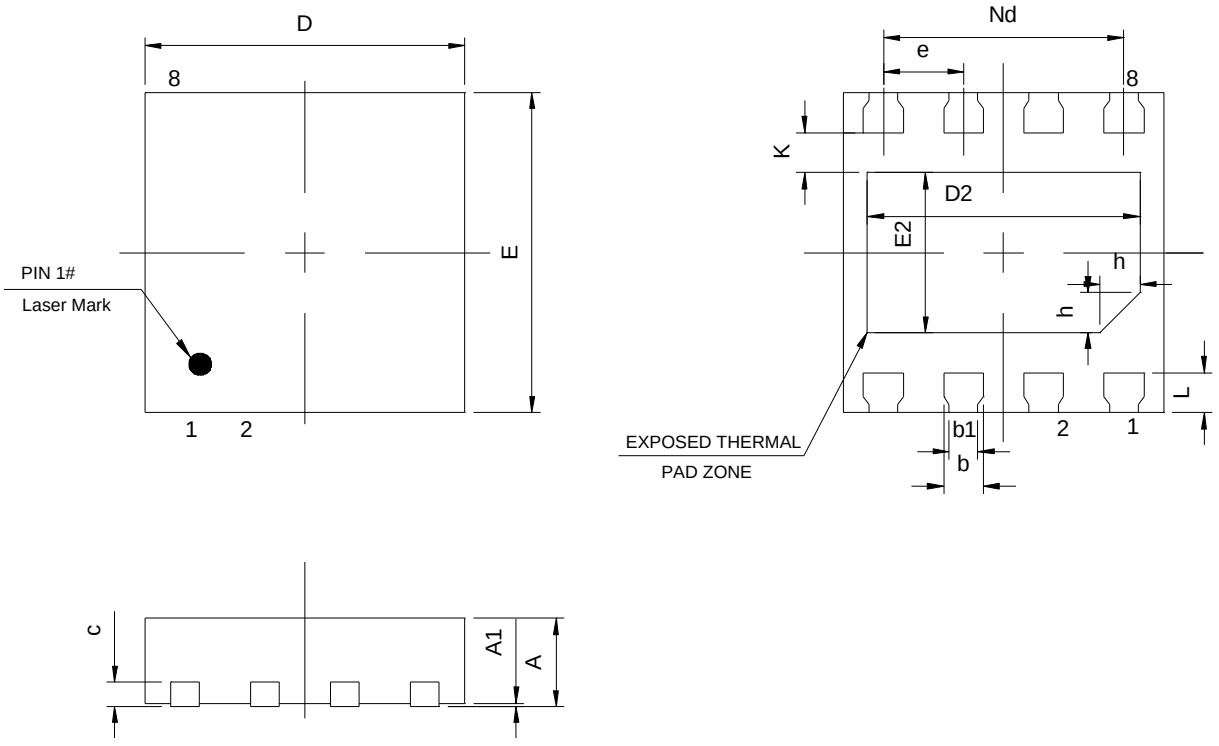
9 Package Information

9.1 Outline Dimensions

DFN8L Package Outline



NOTES:

1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 3 *DFN8L dimensions(mm)*.

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Table 3. DFN8L dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.50	0.55	0.60
A1	0	0.02	0.05
b	0.20	0.25	0.30
b1	0.18REF		
c	0.152REF		
D	1.90	2.00	2.10
D2	1.60	1.70	1.80
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.50BSC		
h	0.20	0.25	0.30
K	0.25REF		
L	0.20	0.25	0.30
Nd	1.50BSC		

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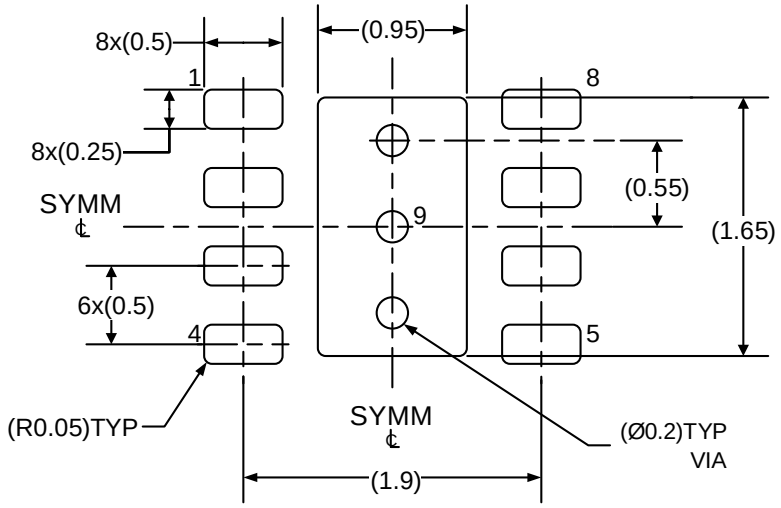
9.2 Recommended Land Pattern

DFN8L Land Pattern Example



NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 20X scale.

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10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30SP2201WETR-I	DFN8L	Green	Tape & Reel	3000	−40°C to +85°C

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11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Initial release and device details	2023

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