Single-Cell Li-ion Battery Charger with Power Path Management

1 Features

- Fully Charger Cycle for Single-Cell Li-Ion/Polymer Batteries, 3.6V to 4.54V Can be Programmed
- Charging Current up to 456mA
- High Charge Voltage Accuracy +/-0.5%
- I2C Interface for Setting Charging Parameters and Status Reporting
- No External Blocking Diode Required
- System Reset Function
- Built-in Battery Disconnection Function for Shipping Mode
- 36V Maximum Input Rating with Over Voltage Protection (OVP)
- Input Under-Voltage Lockout Protection
- Input Over Current Protection
- System Short Circuit Protection
- Over-Discharge Current Protection
- Thermal Shutdown
- PCB Over-Temperature Protection
- Available in a WLCSP-9 Package

2 Applications

- TWS earbuds charging case
- Headsets and hearing aids
- Fitness Accessories
- Smart Watches

3 Description

The GD30WS8663 is a highly integrated Li-ion charger IC for wearable and IoT applications. The IC integrates a high accuracy linear charger of programmable charging current (up to 456mA).

The device integrates advanced power path management and control that allows the device to provide power to the system while charging the battery even with poor adapters. The dynamic power path management is able to automatically balance the currents delivered to the system and battery charging. A high voltage and over current protection circuit is implemented in the IC to protect it from high input voltage as high as 36V.

The GD30WS8663 device supports charge current up to 456mA and supports termination current down to 1mA. The maximum charge current is set at a default of 128mA and is programmable via I2C. The battery is charged using a standard Li-ion charge profile with three phases: pre-charge, constant current and constant voltage regulation.

The device has several power saving modes to increase battery life whether the product is in storage or in operation.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
GD30WS8663	WLCSP-9	1.750 mm x 1.750 mm

1. For packaging details, see *Package Information* section.

Simplified Application Schematic

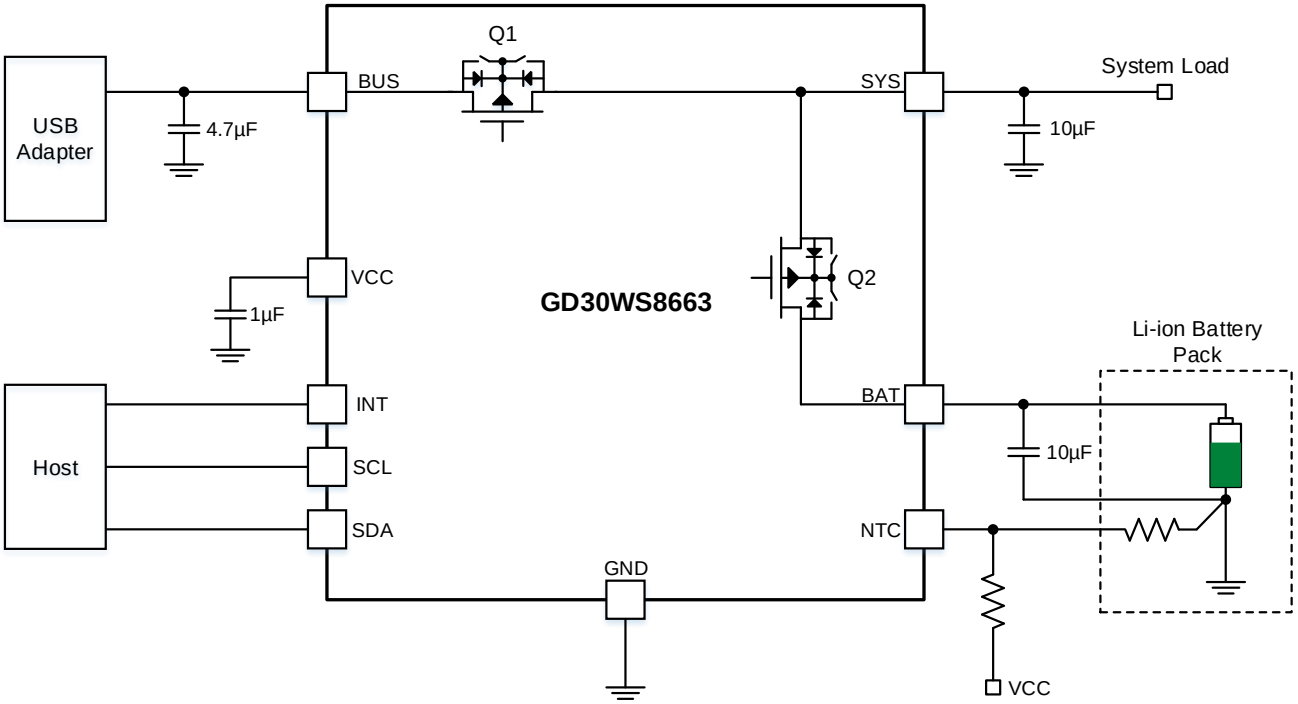
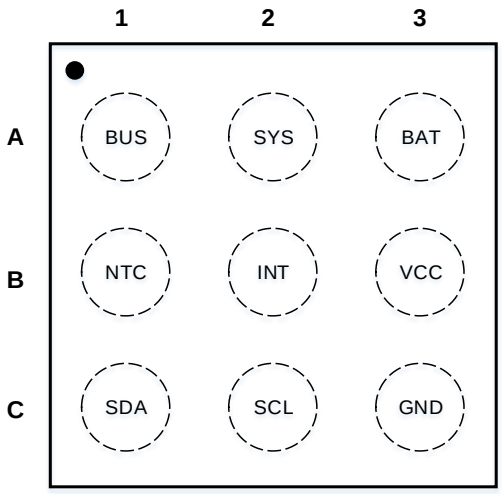


Table of Contents

4 Device Overview

4.1 Pinout and Pin Assignment

WLCSP-9
(Top View)



4.2 Pin Description

PINS		PIN TYPE[1]	FUNCTION
NAME	NUM		
BUS	A1	P	Input power pin. Power input from BUS or other 5V voltage source. Connect a ceramic capacitor from BUS to GND as close to IC as possible.
SYS	A2	P	System power supply. Connect a ceramic capacitor from SYS to GND as close to IC as possible.
BAT	A3	P	Battery pin. Connect to battery positive node. Connect a ceramic capacitor from BAT to GND as close to IC as possible.
NTC	B1	I/O	Temperature sense input. Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VCC to NTC to GND. Charging is suspended when NTC is out of the range. Disabled by writing *REG06H* Bit7= 0 is not used.
INT	B2	I/O	Open drain interrupt output. Send charge status and fault interruption to host.
VCC	B3	P	Internal control power supply pin. LDO output voltage, connect a 1μF ceramic capacitor from VCC to GND.
SCL	C1	I/O	I2C communication from/to the host controller, clock.
SDA	C2	O	I2C communication to the host controller, data.
GND	C3	G	Ground.

1. O = Output, I/O = Input or Output, P = Power, G = Ground.

5 Parameter Information

5.1 Absolute Maximum Ratings

Exceeding the operating temperature range (unless otherwise noted)[1,2]

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{BUS}	Power supply pin from BUS other 5V input	−0.3	36	V
V_{BAT}	Battery voltage	−0.3	7	V
V_{SYS}	System Voltage	−0.3	7	V
V_{CC}	LDO output voltage	−0.3	7	V
V_{IO}	Internal logic voltage (NTC, INT, SCL, SDA)	−0.3	7	V
T_J	Operating junction temperature,	−40	150	°C
T_{stg}	Storage temperature,	−65	150	°C

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values are with respect to network ground terminal.

5.2 Recommended Operation Conditions

SYMBOL[1]	PARAMETER	MIN	TYP	MAX	UNIT
V_{BUS}	Power supply pin from BUS other 5V input	4.35		5.5	V
V_{BAT}	Battery voltage			4.65	V
V_{SYS}	System Voltage	4.2		5	V
V_{IO}	Internal logic voltage (NTC, INT, SCL, SDA)	3.15			V
T_J	Operating Junction temperature[2]	−40		125	°C

1. The device is not guaranteed to function outside of its operating conditions.
2. Power dissipation and thermal limits must be observed.
3. When the device is in shipping mode, the maximum VCC is max(V_{BUS}, V_{BAT}), and the maximum VCC is 3.45V in other modes.

5.3 Electrical Sensitivity

SYMBOL	CONDITIONS	VALUE	UNIT
$V_{ESD(HBM)}$	Human-body model (HBM), ANSI/ESDA/JEDEC JS-001-2017[1]	±2000	V
$V_{ESD(CDM)}$	Charge-device model (CDM), ANSI/ESDA/JEDEC JS-002-2022[2]	±1000	V

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.4 Thermal Resistance

SYMBOL[1]	CONDITIONS	WLCSP-9	UNIT
Θ_{JA}	Natural convection, 2S2P PCB	69.16	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	15.25	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	13.16	°C/W

1. Thermal characteristics are based on simulation, and meet JEDEC document JESD51-7.

5.5 Electrical Characteristics

V_{BUS} = 5V or V_{BAT} = 5V, T_A = +25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SOURCE AND BATTERY PROTECTION						
V_{BUS_UVLO}	V_{BUS} under-voltage lockout threshold	V_{BUS} falling	3.62	3.73	3.82	V
	V_{BUS} under-voltage lockout threshold hysteresis	V_{BUS} rising		170		mV
V_{BUS_OVP}	V_{BUS} over-voltage protection threshold	VBUS rising threshold	5.85	6	6.15	V
	V_{BUS} over-voltage protection threshold hysteresis			340		mV
V_{HDRM}	V_{BUS} vs. battery voltage headroom threshold	VBUS rising vs. battery	80	130	170	mV
	V_{BUS} vs. battery voltage headroom threshold hysteresis			65		mV
V_{BAT_UVLO}	Battery under-voltage lockout threshold	V_{BAT} voltage falling, REG01H[2:0] =000	2.35	2.45	2.55	V
		V_{BAT} voltage falling, REG01H[2:0] =100	2.75	2.85	2.95	
		V_{BAT} voltage falling, REG01H[2:0] =111	3.05	3.15	3.25	
V_{BAT_UVLO}	Battery under-voltage threshold hysteresis	V_{BAT_UVLO} = 2.85V		190		mV
V_{BAT_OVP}	Battery over-voltage protection threshold	Rising, higher than V_{BAT_REG}		130		mV
	Battery over-voltage protection hysteresis			65		
POWER PATH MANAGEMENT						
$V_{SYS\_REG\_ACC}$	Regulated system output voltage accuracy	V_{BUS} = 5.5V, RSYS = 100Ω, I_{CHG} = 0A, REG07H[3:0] = 0000, V_{SYS_REG} = 4.2V	−2		2	%
		V_{BUS} = 5.5V, RSYS = 100Ω, I_{CHG} = 0A, REG07H[3:0] = 1001, V_{SYS_REG} = 4.65V	−2		2	
		V_{BUS} = 5.5V, RSYS = 100Ω, I_{CHG} = 0A, REG07H[3:0] = 1111, V_{SYS_REG} = 4.95V	−2		2	

Typical Application Curves (continued)

V_{BUS} = 5V or V_{BAT} = 5V, T_A = +25°C, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{BUS_LIM}	V_{BUS} current limit	REG00H[3:0] = 0000, I_{BUS_LIM} = 50mA	40	50	60	mA
		REG00H[3:0] = 0011, I_{BUS_LIM} = 140mA	125	140	155	
		REG00H[3:0] = 1001, I_{BUS_LIM} = 320mA	295	320	345	
		REG00H[3:0] = 1111, I_{BUS_LIM} = 500mA	455	500	545	
V_{BUS_MIN}	V_{BUS} minimum voltage regulation	REG00H[7:4] = 0000, V_{BUS_MIN} = 3.88V	3.68	3.88	4.18	V
		REG00H[7:4] = 1001, V_{BUS_MIN} = 4.60V	4.40	4.60	4.75	
		REG00H[7:4] = 1111, V_{BUS_MIN} = 5.08V	4.88	5.08	5.35	
R_{ON_Q1}	BUS to SYS switch on resistance	V_{BUS} = 4.5V, I_{SYS} = 100mA		290		mΩ
I_{BUS_Q}	V_{BUS} quiescent current	V_{BUS} = 5.5V, EN_HIZ = 0, CEB = 0, charge enable, I_{CHG} = 0A, I_{SYS} = 0A		2.1		mA
		V_{BUS} = 5.5V, EN_HIZ = 0, CEB = 1, charge disabled		1.9		
I_{BAT_Q}	Battery quiescent current	V_{BUS} = 5V, CEB = 0, I_{SYS} = 0A, charge done, V_{BAT} = 4.35V		15		μA
		V_{BUS} = GND, CEB = 1, I_{SYS} = 0A, V_{BAT} = 4.35V, disable PCB_OTP function, not including the current from the external NTC resistor		6.5	8.5	
		V_{BUS} = GND, CEB = 1, I_{SYS} = 0A, V_{BAT} = 4.35V, enable PCB_OTP function, not including the current from the external NTC resistor		14.5	22	
		V_{BAT} = 4.5V, V_{BUS} = V_{SYS} = GND, FET_DIS = 1, shipping mode			200	nA
R_{ON_Q2}	B-FET on resistance	V_{BUS} < 2V, V_{BAT} = 3.5V, I_{SYS} = 100mA		100		mΩ
I_{DSG}	B-FET discharge current limit	REG03H[7:4] = 0001		400		mA
		REG03H[7:4] = 1001		2000		
V_{FWD}	Ideal diode forward voltage in supplement mode	50mA discharge current		23		mV
SHIPPING MODE						
t_{SMEN_DGL}	Enter shipping mode deglitch time	REG09H[7:6] = 00		1		s
t_{SMEX_DGL}	Exit shipping mode by INT or BUS plug-in	INT is pulled low		2		s

Typical Application Curves (continued)

V_{BUS} = 5V or V_{BAT} = 5V, T_A = +25°C, unless otherwise noted.

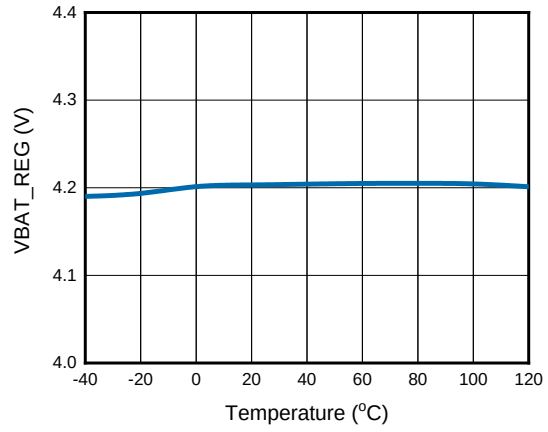
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
AUTO-RESET MODE						
t_{RST_DGL}	Reset by INT	REG01H[7:6] = 00		8		s
		REG01H[7:6] = 10		16		
t_{RST_DUR}	BFET off lasting time	REG01H[5] = 0		2		s
		REG01H[5] = 1		4		
BATTERY CHARGER						
V_{BAT_REG}	Battery charge voltage regulation	REG04H[7:2] = 000000, V_{BAT_REG} = 3.6V	3.582	3.6	3.618	V
		REG04H[7:2] = 101000, V_{BAT_REG} = 4.2V	4.188	4.2	4.212	
		REG04H[7:2] = 110010, V_{BAT_REG} = 4.35V	4.358	4.35	4.44	
		REG04H[7:2] = 111110, V_{BAT_REG} = 4.53V	4.522	4.53	4.552	
I_{CC}	Constant current	REG02H[5:0] = 001111, I_{CC} = 128mA	113	128	137	mA
		REG02H[5:0] = 111000, I_{CC} = 456mA	424	456	488	
T_{J_REG}	Junction temperature regulation	Thermal_Limit = 120°C		120		°C
I_{PRE}	Pre-charge current	I_{PRE}=5% * ICC, I_{CC_Finer}=25% * I_{CC}, REG0C[0]=1		5% * I_{CC}		mA
I_{TERM}	Charge termination current threshold	REG03H[3:0] = 0000, I_{TERM} = 1mA		0.95		mA
		REG03H[3:0] = 0001, I_{TERM} = 3mA		3.05		
		REG03H[3:0] = 0101, I_{TERM} = 11mA		11		
		REG03H[3:0] = 0101, I_{TERM} = 31mA		31		
V_{BAT_PRE}	Pre-charge to constant current charge threshold	V_{BAT} rising, REG04H[1] = 1, V_{BAT_PRE} = 3.0V	2.9	3	3.1	V
	Pre-charge to constant current charge threshold hysteresis			320		mV
V_{RECH}	Battery auto-recharge voltage threshold	Below V_{BAT_REG}, REG04H[0] = 0	55	100	145	mV
		Below V_{BAT_REG}, REG04H[0] = 1	155	200	245	
THERMAL PROTECTION						
T_{J_SHDN}	Thermal shutdown threshold			150		°C
	Thermal shutdown hysteresis			20		
I_{NTC}	NTC output current	CEB = 0, NTC = 3V	−1	0	1	μA
V_{COLD}	NTC cold temp rising threshold	As a percentage of VCC		76		%
	NTC cold temp rising threshold hysteresis			60		mV

Typical Application Curves (continued)

V_{BUS} = 5V or V_{BAT} = 5V, T_A = +25°C, unless otherwise noted.

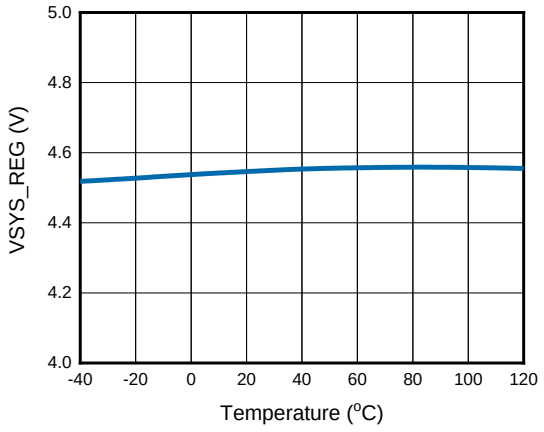
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{COOL}	NTC cool temp rising threshold	As a percentage of VCC		61		%
V_{HOT}	NTC hot temp falling threshold	As a percentage of VCC		30		%
	NTC hot temp falling threshold hysteresis			70		mV
V_{HOT_PCB}	NTC hot temp falling threshold for PCB_OTP	As a percentage of VCC		30		%
	NTC hot temp falling threshold hysteresis for PCB_OTP			90		mV
LOGIC INPUT PIN CHARACTERISTICS						
V_{IL}	Input logic low voltage		0		0.8	V
V_{IH}	Input logic high voltage		1.5		5.5	V
V_{HYS}	Input logic hysteresis		100			mV
OPEN DRAIN OUTPUT CHARACTERISTICS						
V_{INT}	Output logic low voltage	I_O = 5 mA			0.1	V
V_{SDA}	Output logic low voltage	I_O = 5 mA			0.1	V
I_{OD}	Output high impedance leakage	V_O = 5 V	−2		2	μA
WATCHDOG TIMER						
t_{WDT}	Watchdog timer	REG05H[6:5] = 11		160		s

5.6 Typical Characteristics



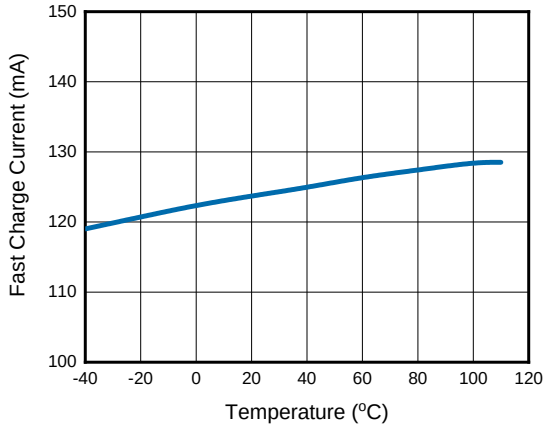
V_{BAT} = 4.2V

Figure 1. VBAT Regulation Voltage vs. Temperature



V_{SYS} = 4.55A

Figure 2. VSYS Regulation Voltage vs. Temperature



I_{OUT} = 128mA

Figure 3. Fast Charge Current vs. Temperature

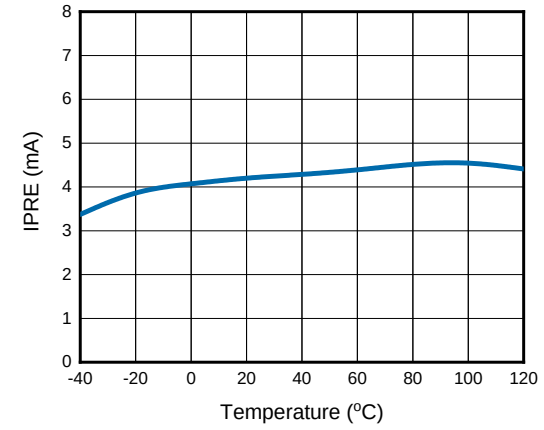
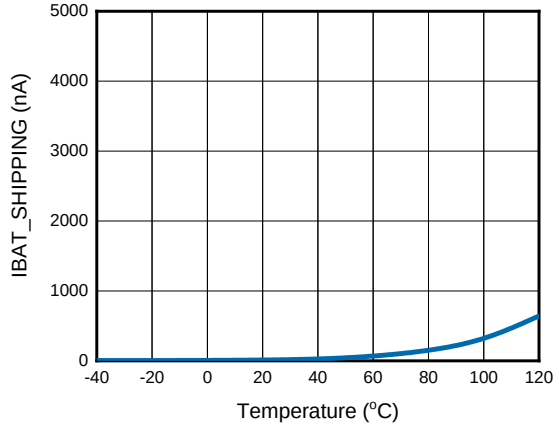
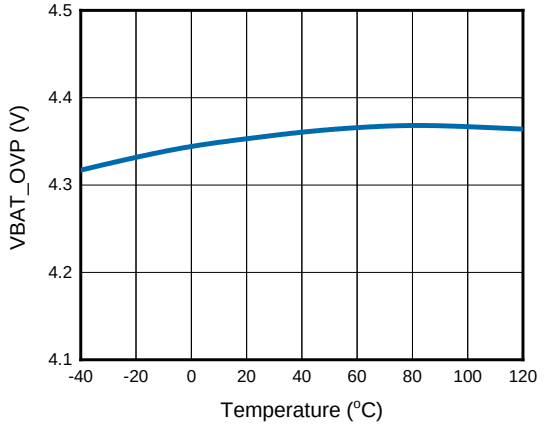


Figure 4. Pre-Charge Current vs. Temperature



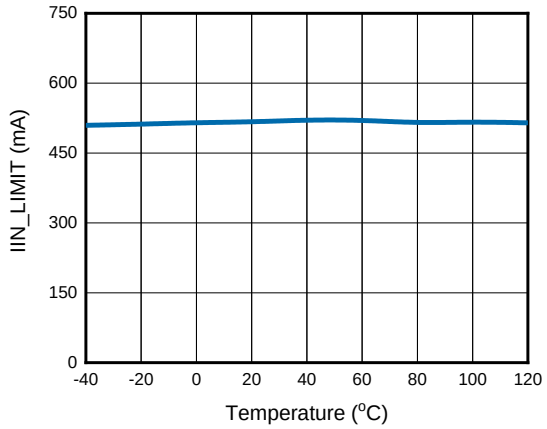
Shipping Mode

Figure 5. Battery Current vs. Temperature



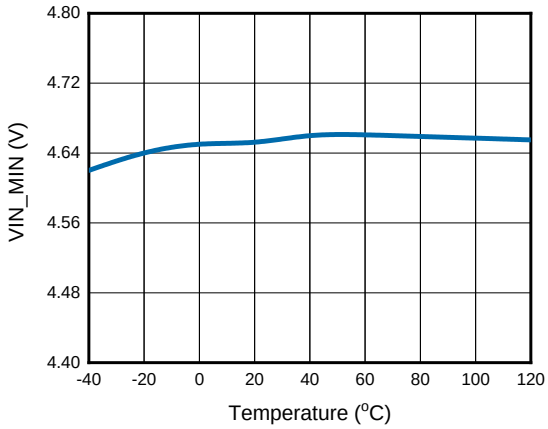
V_{BAT} = 4.2V

Figure 6. Battery OVP Voltage vs. Temperature



I_{IN_LIM} = 500mA

Figure 7. Input Current Limit vs. Temperature



V_{IN_MIN} = 4.60A

Figure 8. Input Minimum Voltage vs. Temperature

6 Functional Description

6.1 Block Diagram

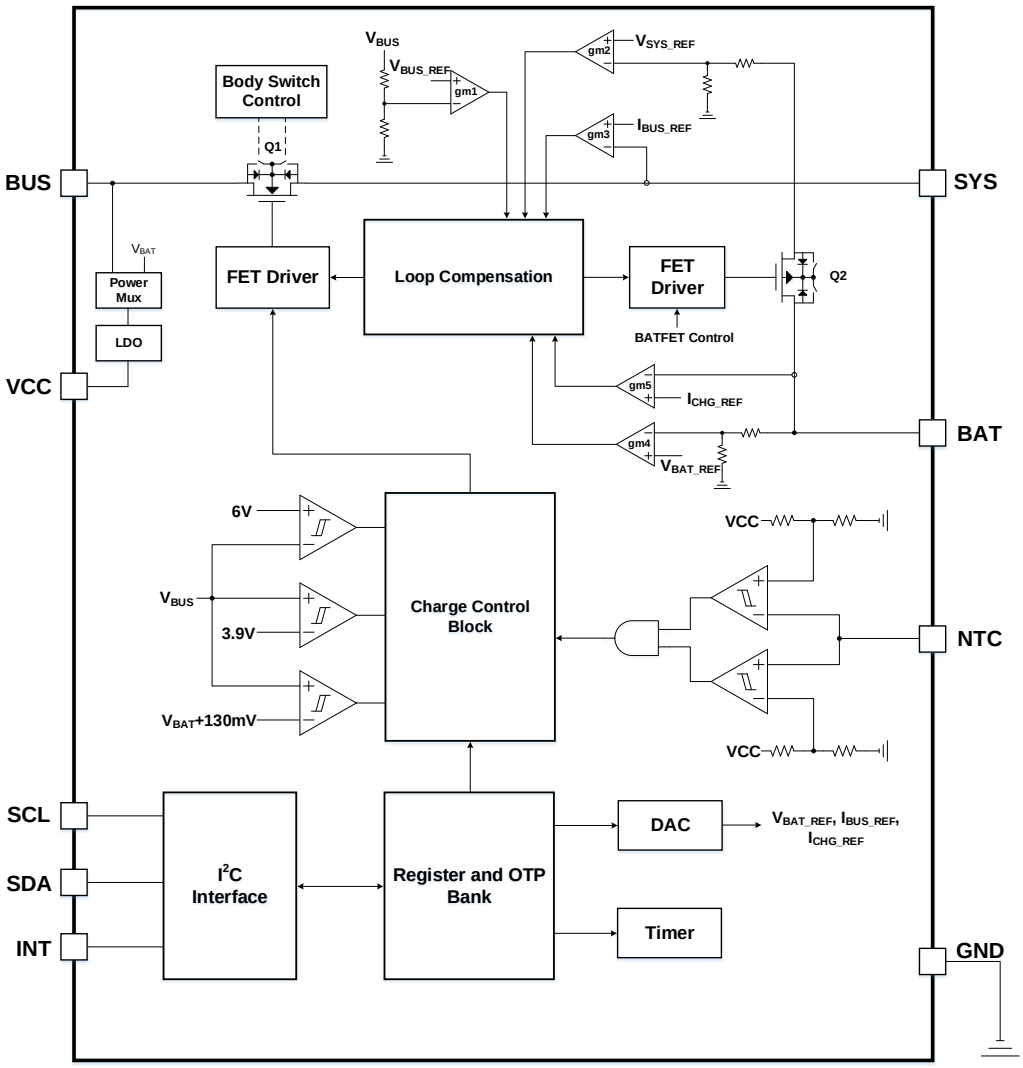


Figure 9. GD30WS8663 Functional Block Diagram

6.2 Operation

The GD30WS8663 is a highly integrated Li-ion charger IC for wearable and IoT applications. The IC integrates a high accuracy linear charger of programmable charging current (up to 456mA). The device also includes power path management and high input protection functions.

The device integrates advanced power path management and control that allows the device to provide power to the system while charging the battery even with poor adapters. The dynamic power path management is able to automatically balance the currents delivered to the system and battery charging. A high voltage and over current protection circuit is implemented in the IC to protect it from high input voltage as high as 36V.

The GD30WS8663 device supports charge current up to 456mA and supports termination current down to 1mA. The maximum charge current is set at a default of 128mA and is programmable via I2C. The battery is charged

using a standard Li-Ion charge profile with three phases: pre-charge, constant current and constant voltage regulation.

The device has several power saving modes to increase battery life whether the product is in storage or in operation.

The versatile features of GD30WS8663 allow for it to best used in wearable applications such as headsets, earbuds and hearing aids, or low battery applications such as smart watches and fitness accessories, or patient monitors and portable medical equipment.

The GD30WS8663 has three different operation modes: shipping, battery operation and BUS operation mode, as shown in Figure 10. The mode of operation is saved in REG08H bit [4:0].

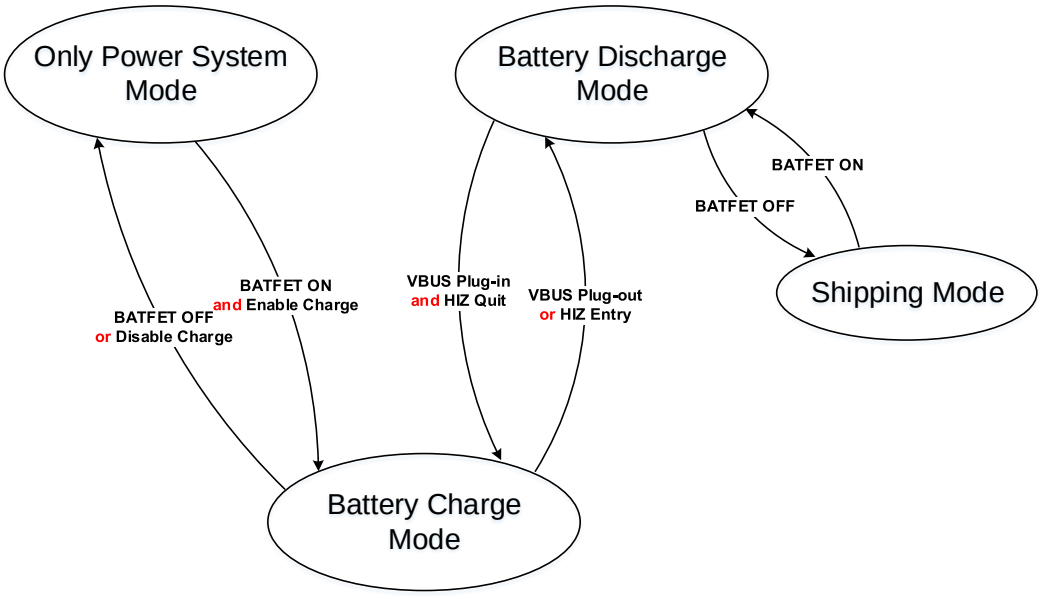


Figure 10. GD30WS8663 Operation Modes

6.2.1 Power Supply

The internal bias circuit of the IC is powered from the higher voltage of either BUS or BAT. When BUS or BAT rises above its respective under-voltage (UVLO) threshold, the sleep comparator, battery depletion comparator, and BATFET(Q2) driver are all active. The I2C interface is ready for communication, and all register are reset to the default value. The host can access all of the register.

6.2.2 Battery Charge

The GD30WS8663 device integrates a linear charger that allows the battery to be charged with a programmable charge current up to 456mA. In addition to the charge current, other charging parameters can be also programmed through I2C such as the battery regulation voltage, pre-charge current and termination charge current. The device supports multiple battery regulation voltage regulation settings (VREG) and charge current (I_{CHG}) options to support multiple battery chemistries for single-cell applications. A full one-cell linear charger state diagram as shown in Figure 11 is implemented in the IC.

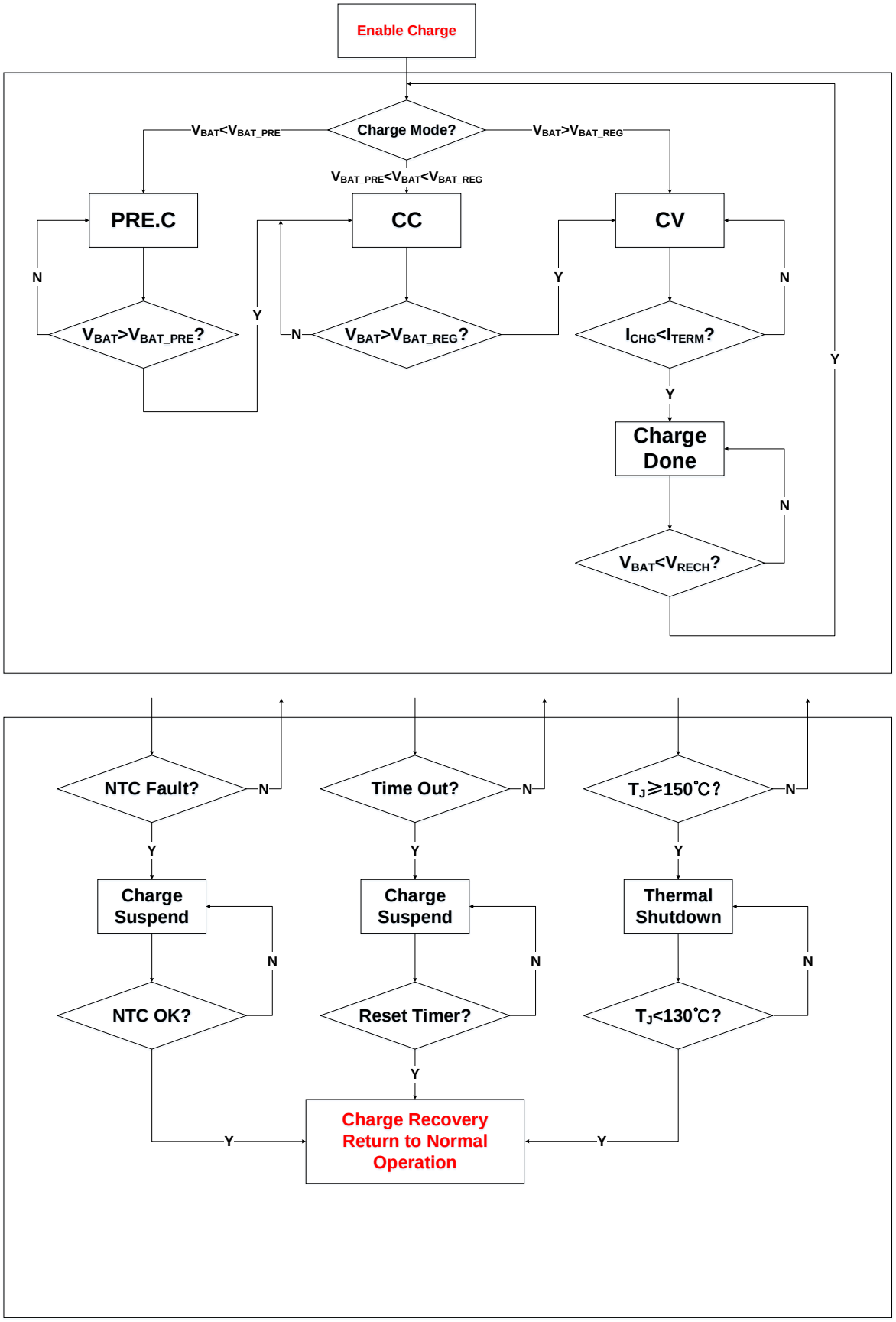


Figure 11. Battery Charge State Diagram

The GD30WS8663 provide three main charging phases: Pre-charge, Constant current charge and constant voltage charge in Figure 12.

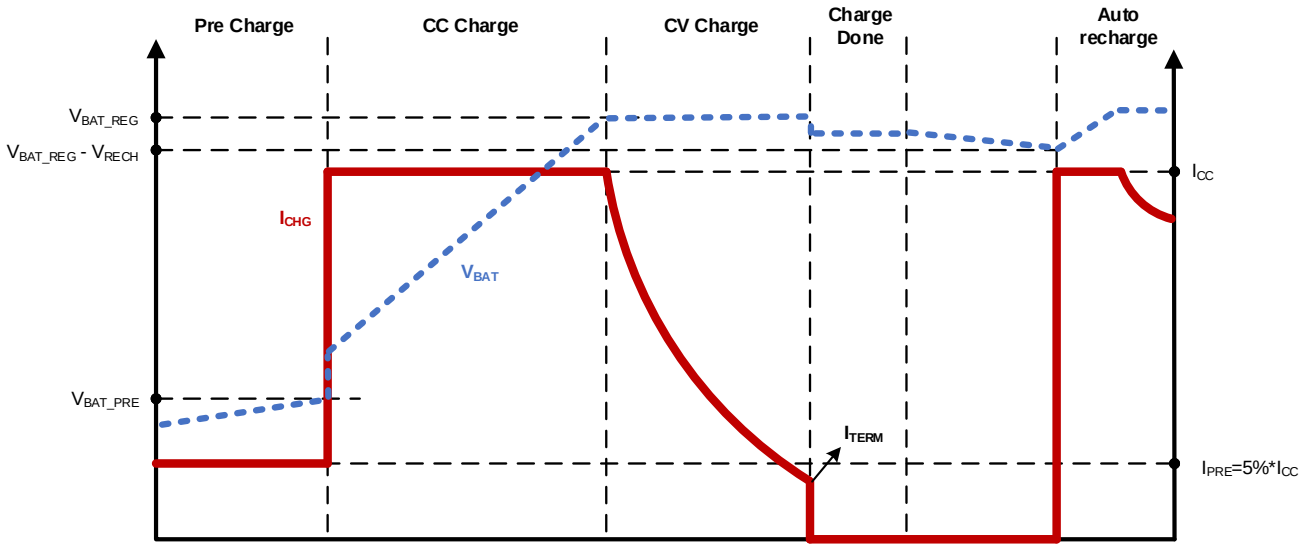


Figure 12. Battery Charge Cycle and Charge Parameters

Phase 1 (pre-charge): The GD30WS8663 can safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to constant current threshold(V_{BAT_PRE}). The pre-charge current is equal to 5% of the I_{CC}. If V_{BAT_PRE} is not reached before the pre-charge timer (1h) expires, the charge cycle stop, and a corresponding timeout fault signal is asserted.

Phase 2 (constant-current charge): When the battery voltage exceeds V_{BAT_PRE}, the GD30WS8663 enters a constant current charge phase. The phase charge current can be programmed via REG02H bit [5:0].

Phase 3 (constant-voltage charge): When the battery voltage rises to the battery-full voltage(V_{BAT_REG}) set via REG04H bit [7:2], the charge mode changes from CC mode to CV mode, and the charge current starts decreasing.

The charger input has back to back blocking FETs to prevent reverse current flow from BAT to BUS. They also integrate control circuitry regulating the input current and prevents excessive currents from being drawn from the input power supply for more reliable operation.

Assuming that the termination function EN_TERM is set via REG05H bit [4] = 1, the charge cycle is considered to be completed when the charge current (I_{CHG}) reaches the termination current threshold (I_{TERM}). The charge status is immediately updated to charge done.

The termination charge current threshold (I_{TERM}) can be programmed via REG03H bit [3:0]. If EN_TERM = 0, the termination function is disable and all of the above actions are invalid (see Table 1).

Table 1. Termination Function Selection Table

EN_TERM	TERM_TMR	After I_{BAT} Reaches I_{TERM} in CV Mode	
		Operation	Charge status
0	x	Keep CV Charge	Charge
1	0	Charge done	Charge done
1	1	Keep CV Charge	Charge

1. Type: x = Don't Care.

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation.

A new charge cycle starts when any of the following conditions are valid:

- The input power is recycled.
- Battery charging is enabled via the I2C.
- Auto-recharge kick in.

Under the following conditions:

- No thermistor fault at NTC.
- No safety timer fault.
- No battery over-voltage event.
- BATFET is not forced off.

6.2.3 Auto Recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharge below the recharge threshold and V_{BUS} is still in the operating range, the GD30WS8663 begins another new charging cycle automatically without having to restart a charging cycle manually. The auto-recharge function is valid only when EN_TERM = 1.

6.2.4 Battery Discharge

If the battery is connected and the input source is missing, the BATFET is fully on when V_{BAT} is above the V_{BAT_UVLO} threshold. The 100mΩ BATFET minimizes conduction loss during discharge. The quiescent current of the GD30WS8663 is as low as 6.5μA in this mode. The low R_{DS_ON} and low IQ help extend the running time of the battery.

6.2.5 Power Path Management and Battery Supplement

The GD30WS8663 employs a pass-through power path structure with the BATFET to decouple the system from the battery. This allows for separate control between the system and the battery. The system is given the priority to start up, even with a deeply discharged or missing battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDOFET. The direct power structure consists of a frontend LDOFET between BUS and SYS and a BATFET between SYS and BAT. The LDOFET and BATFET can be controlled by the I2C (see Table 2).

Table 2. FET Control Via I2C

FET ON/OFF Changed by control	Hi-Z Mode and Charge Control	
	Set EN_HIZ to 1	Set CEB to 0
LDOFET	ON	X
BATFET (Charging)	x	ON
BATFET (discharging)	x	X

1. x = Don't Care.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDOFET is fully on with input current limit. V_{SYS_REG} can be programmed through REG07H bit[3:0].

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is reduced to zero and the input source is still overloaded due to a heavy system load, the system voltage begins decreasing. Once the system voltage drops to 30mV below the battery voltage, the GD30WS8663 enters battery supplement mode, and the ideal diode mode is enabled. The BATFET is regulated to keep V_{BAT} - V_{SYS} at 23mV when I_{DSG} (supplement current) * R_{ON_BATFET} is lower than 23mV. In the case that I_{DSG} * R_{ON_BATFET} is higher than 23mV, the BATFET is fully turned on to maintain the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than V_{BAT} + 23mV, the ideal diode mode is disabled, shown in Figure 13.

When V_{BUS} is not available, the GD30WS8663 operates in discharge mode, and the BATFET is always fully on to reduce loss.

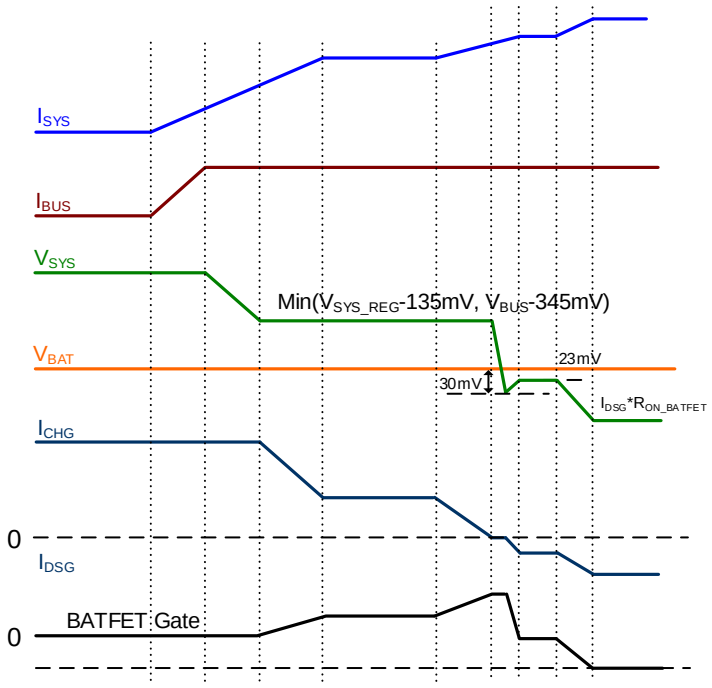


Figure 13. Dynamic Power Management and Battery Supplement Operation Profile

6.2.6 Internal to Host(INT)

The GD30WS8663 also has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256μs or 2.56ms low-state INT pulse. All of the below events can trigger an INT output.

- Good input source detected
- UVLO or input over-voltage protection
- Charge completed
- Charging status change
- Fault in REG08/09H (watchdog timer fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When fault occurs, the GD30WS8663 sends out an INT pulse and latches the fault state in REG08/09H. After the GD30WS8663 exits the fault state, the fault bit is reset to 0 after the host reads REG08/09H. The NTC fault bit is not latched and always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set in REG06H bit [4:0]. When an INT condition is masked, this means that the INT pin signal (and register bit) will not trigged when the corresponding condition occurs. Masking INTs is useful when writing software code to avoid unnecessary interruptions due to these events.

6.2.7 NTC Battery Temperature

NTC allows the GD30WS8663 to sense the battery temperature using the thermistor (usually available in the battery pack) to ensure a safe operating environment for the battery. Connect appropriately valued resistors from VCC to NTC to ground. The resistor divider works with a thermistor connected from NTC to ground. The NTC voltage is determined by the resistor divider whose divide ratio depends on the temperature. The GD30WS8663 sets a pre-determined upper and lower bound of the divide ratio for NTC cold and NTC hot internally.

In the GD30WS8663, the I2C default setting is PCB_OTP. This function can be changed through the I2C (see Table 3).

Table 3. NTC Function Selection Table

I2C Control		Function
EN_NTC	EN_PCB_OTP	
0	x	Disable
1	1	NTC
1	0	PCB_OTP

1. Type: x = Don't Care.

When PCB_OTP is selected and the NTC voltage is lower than the NTC hot threshold, both the LDOFET(Q1) and BATFET are off. The PCB_OTP fault also sets the NTC_FAULT status (REG09H bit [1]) to 1 to show the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function works only in charge mode. Once the NTC voltage falls out of this divide ratio, the temperature is outside of the safe operating range, and the GD30WS8663 stops charging and report it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

6.2.8 System Protection

6.2.8.1 Input OVP and UVLO Protection

The GD30WS8663 has an input over-voltage protection (OVP) threshold and input UVLO threshold. Once the input voltage is out of its normal range, the LDOFET is turned off immediately.

When the input voltage is identified as a good source, an immunity timer becomes active. If the input power is normal until the immunity timer expires, the system starts up. Otherwise, Q1 remains off (see Figure 14).

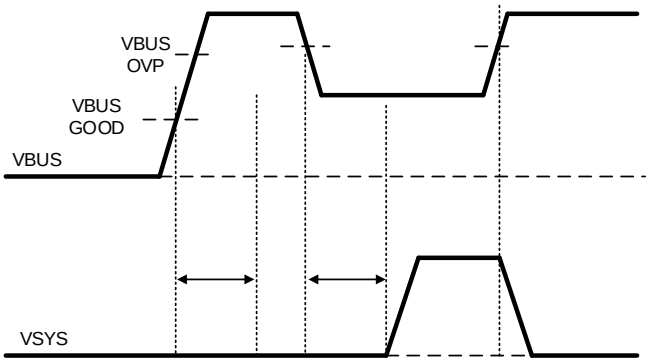


Figure 14. Input Power Detection Operation Profile

6.2.8.2 Battery OVP Protection

The GD30WS8663 is designed with a built-in battery over-voltage limit (about 130mV higher than V_{BAT_REG}). When a battery over-voltage event occurs, the GD30WS8663 suspends charging immediately and asserts a fault.

6.2.8.3 Over-Discharge Current Protection

The GD30WS8663 has an over-discharge current protection in discharge mode and supplement mode. Once IDSG exceeds the programmable discharge current limit (2A default), the BATFET turns off after a 60μs delay. The GD30WS8663 enters hiccup mode as part of the over-current protection (OCP). The discharge current limit can be programmed high to 3.2A through the I2C. If the discharge current goes high and reaches the internal fixed current limit (about 3.7A), the BATFET turns off and begins hiccup mode immediately. Similarly, when the battery voltage falls below the programmable V_{BAT_UVLO} threshold (2.76V default), the BATFET turns off to prevent an over-discharge.

6.2.8.4 System Short-circuit Protection

The GD30WS8663 features SYS node short-circuit protection (SCP) for both the BUS to SYS path and the BAT to SYS path.

The system voltage is monitored continuously. If V_{SYS} is lower than 1.5V, system SCP for both the BUS to SYS path and the BAT to SYS path is active. I_{DSG} decreases to half of the original value.

For the BUS to SYS path, once I_{BUS} is over the protection threshold, both the LDOFET and BATFET are turned off immediately, and the GD30WS8663 enters hiccup mode. Otherwise, the maximum current limit is not reached. When V_{SYS} is lower than 1.5V and the setting input current limit is reached, the hiccup mode also starts after a 60μs delay. The hiccup mode interval is 800μs.

For the BAT to SYS path, once IBAT is over the 3.7A protection threshold, both the LDOFET and BATFET are turned off immediately, and the GD30WS8663 enters hiccup mode. When the battery discharge current limit

threshold is reached, hiccup mode starts after a 60μs delay. The hiccup mode interval is 800μs.

Particularly, if a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths works. The faster one of the two dominates the hiccup operation. For details, please refer to the flow chart shown in Figure 15.

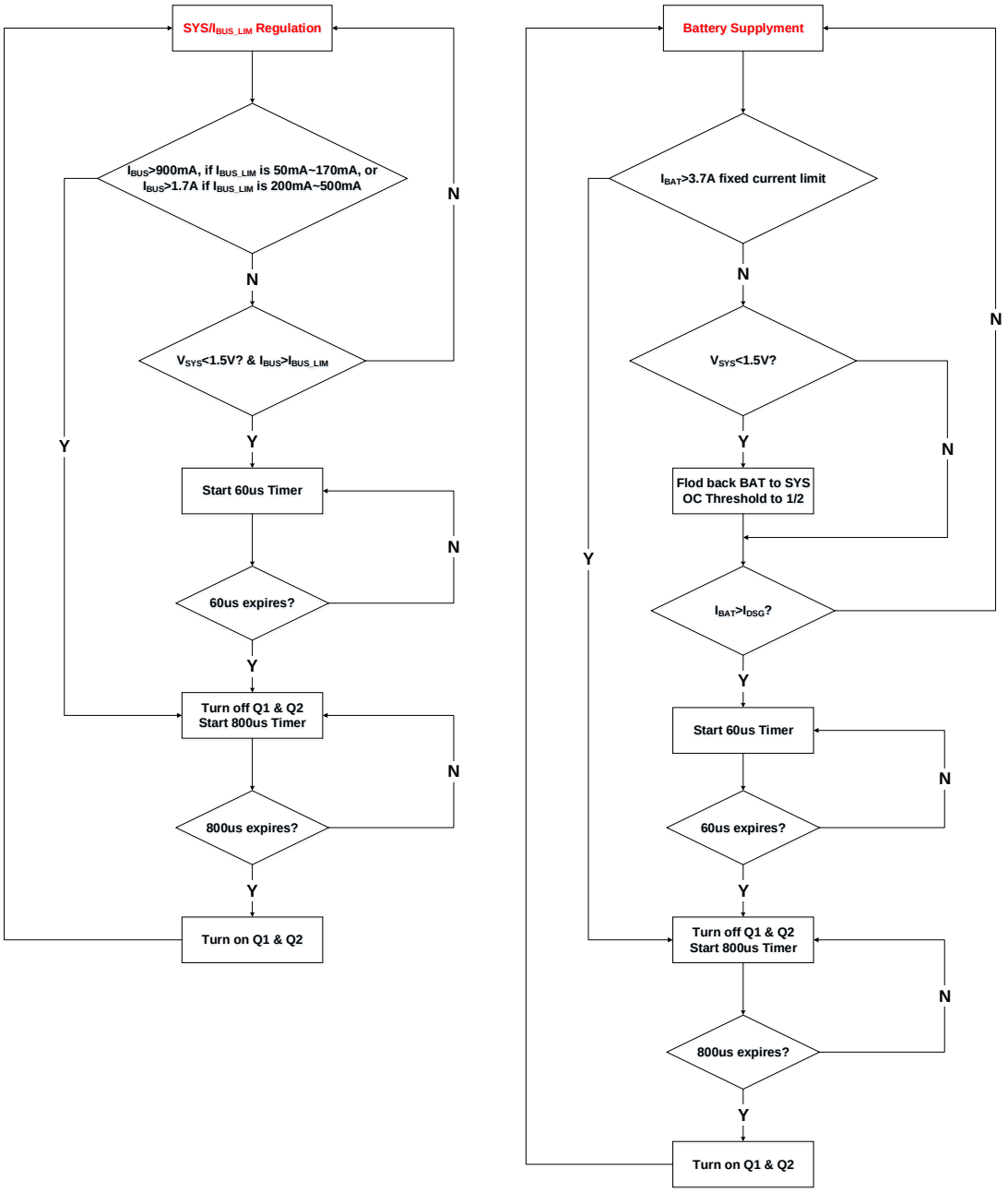


Figure 15. System Short-Circuit Protection

6.2.8.5 Over temperature protection

The GD30WS8663 monitors the internal junction temperature continuously to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset limit of T_{J_REG} (120°C default), the IC starts to reduce the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirements in different applications. The junction temperature regulation threshold can be set via REG03H bit [5:4]. When the junction temperature

reaches 150°C, both Q1 and Q2 turn off.

6.2.9 Safety Timer

The GD30WS8663 provides both a pre-charge and constant current charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer is 1hr when the battery voltage is lower than V_{BAT_PRE}. The constant current(CC) charge safety timer starts when the battery enters CC charge mode. The CC charge safety timer can be programmed through the I2C. The safety timer can be disabled via the I2C.

The following actions can restart the safety timer.

- A new charge cycle is kicked in.
- Write REG01H bit [3] from 1 to 0 (charge disable to enable).
- Write REG01H bit [4] from 1 to 0 (HIZ enable to disable).

6.3 Host Mode and Default Mode

The GD30WS8663 is a host-controlled device. After the power-on reset, the GD30WS8663 starts up in a watchdog timer expiration state or default mode. All registers are in their default settings.

The watchdog timer works in both charge and discharge mode. When the watchdog timer run out, most registers return to the default value. When the watchdog timer is out in both charge and discharge mode, both the LDOFET and BATFET are turned off. They turn on again automatically after t_{RST_DUR}, which can be programmed by REG01H bit [5].

To save quiescent current during discharge mode, the watchdog timer can be turned off during by setting REG05H bit [7] to 0.

Any write to the GD30WS8663 switches it to host mode. All charge parameters are programmable. If the watchdog timer (REG05H bit [6:5]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to REG02H bit [6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the GD30WS8663 goes back to default mode. The watchdog timer limit can also be programmed or disabled by the host control.

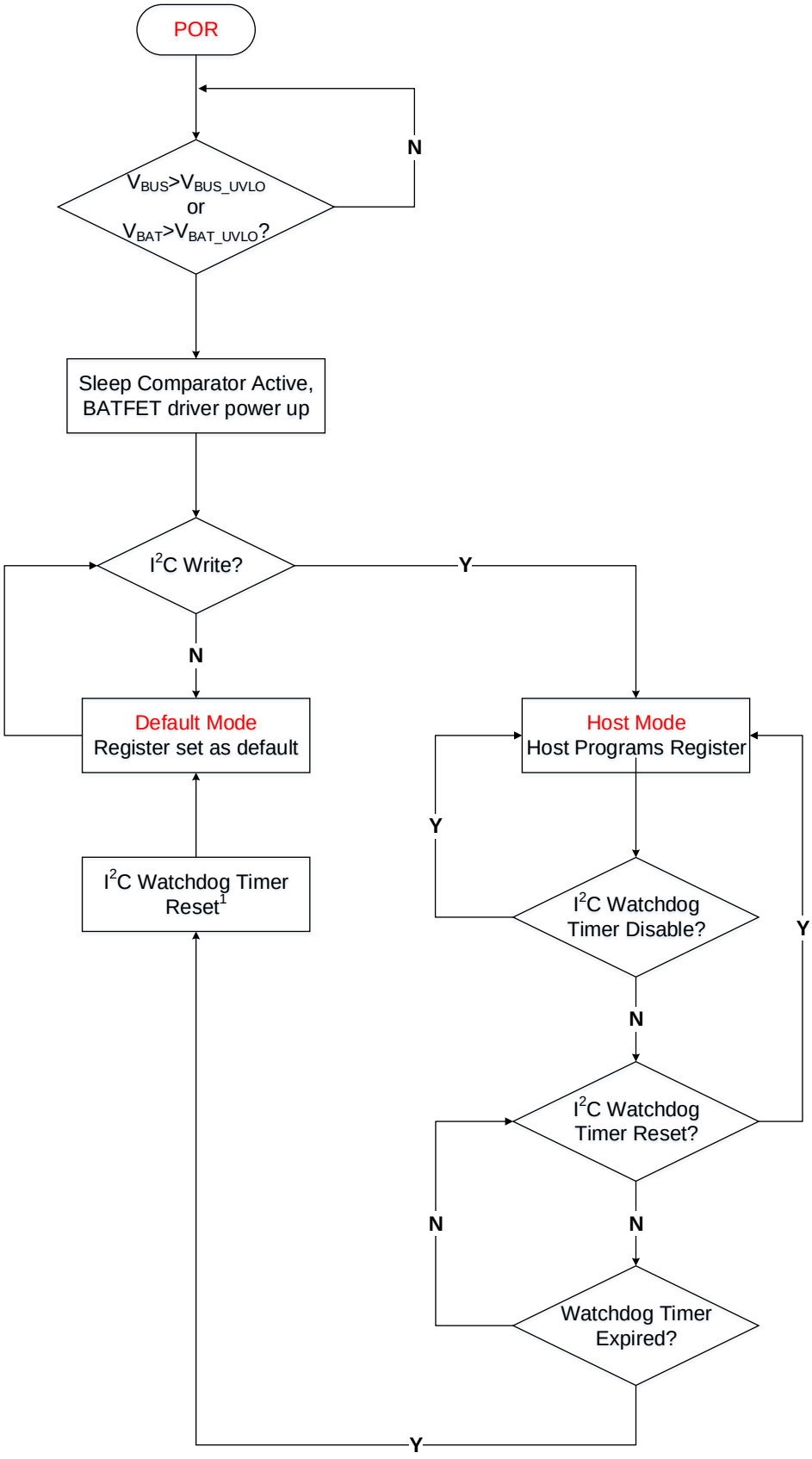


Figure 16. Host Mode and Default Mode Selection

1. Once the watchdog timer expires, the I2C watchdog timer must be reset or will not be valid in the next cycle.

6.4 Shipping Mode

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode or to allow the system power to be reset during the application. The GD30WS8663 provides both shipping mode (shown in Table 4) and system reset mode for different applications.

Table 4. Shipping Mode Control

Items	Enter Shipping Mode	Exit Shipping Mode	
	Set FET_DIS to 1	INT H to L for 2s	V_{BUS} Plug-In
LDOFET	x	x	On
BATFET(Charging)	Off(t_{SMEN_DGL} later)	On	On(2s later)
BATFET(Discharging)	Off(t_{SMEN_DGL} later)	On	On(2s later)

1. Type: x = Don't Care.

The GD30WS8663 has a register bit for battery disconnection control (FET_DIS). If this bit is set to 1, the GD30WS8663 enters shipping mode after a delay time, which can be programmed by REG09H bit [7:6]. The BATFET turns off, and the FET_DIS bit refreshes to 0 after the BATFET turns off. Pull the INT pin down or plug in the input adapter for 2s to wake the GD30WS8663 up from shipping mode.

The GD30WS8663 can also reuse an INT pin to cut off the path from the battery to the system under the condition needed to reset the system manually. Once the logic at INT is set low for longer than t_{RST_DGL} (which can be programmed by REG01H bit [7:6]), the battery is disconnected from the system by turning off the BATFET. The off state lasts for t_{RST_DUR}, which can be programmed by REG01H bit [5]. Then the BATFET is turned on automatically, and the system is powered by the battery again. During the off period, the INT pin is not limited to be high or low.

When the IC exits shipping mode, only registers that can be reset by the watchdog can be reset.

The GD30WS8663 can reset the system by controlling the INT pin (see Figure 17).

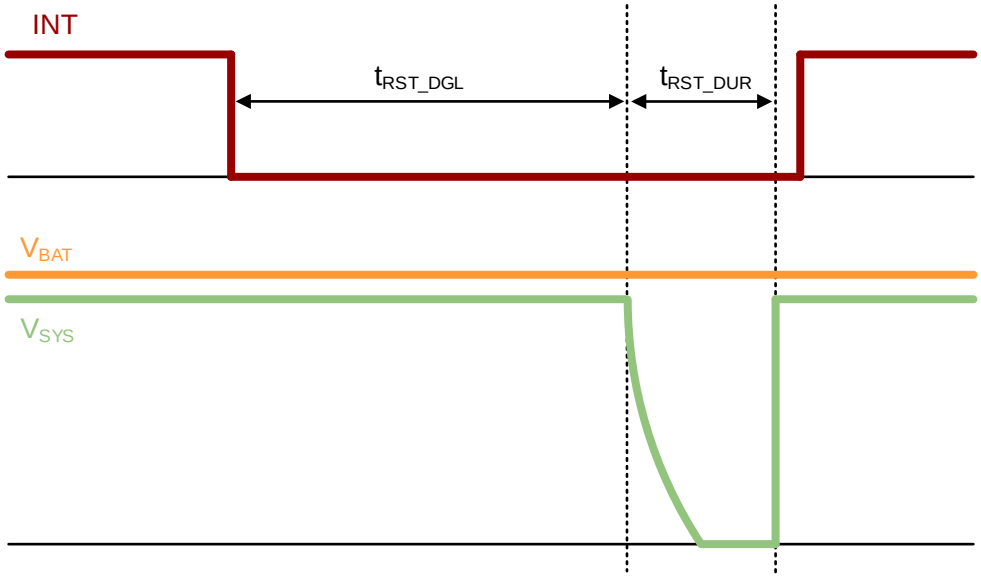


Figure 17. System Reset Function Operation Profile

6.5 I2C Interface

The GD30WS8663 device uses a fully compliant I2C interface to program and read control parameters, status bits, and so on. I2C is a 2-wire serial interface developed by Philips Semiconductor (see I2C-Bus Specification, Version 2.1, January 2000). The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. When the bus is idle, both SDA and SCL lines are pulled high. All the I2C compatible devices connect to the I2C bus through open drain I/O pins, SDA and SCL. A master device, usually a micro-controller or a digital signal processor, controls the bus. The master is responsible for generating the SCL signal and device addresses. The master also generates specific conditions that indicate the START and STOP of data transfer. A slave device receives and/or transmits data on the bus under control of the master device.

The GD30WS8663 7-bit slave address (A7-A1) is 0000111 binary(0x07H). After the START condition, the I2C master sends the 7-bit chip address followed by an eighth (A0) read or write bit ($R/\overline{W}$). $R/\overline{W}$ = 0 indicates a WRITE function and $R/\overline{W}$ = 1 indicates a READ function.

Table 5. Device Address

A7(MSB)	A6	A5	A4	A3	A2	A1	A0(LSB)
0	0	0	0	1(dynamic)	1(dynamic)	1(dynamic)	$R/\overline{W}$

The I2C interface supports both standard mode (up to 100kbits), and fast mode (up to 400kbits). Both SDA and SCL are bi-direction lines, connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain. The Data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred (see Figure 18).

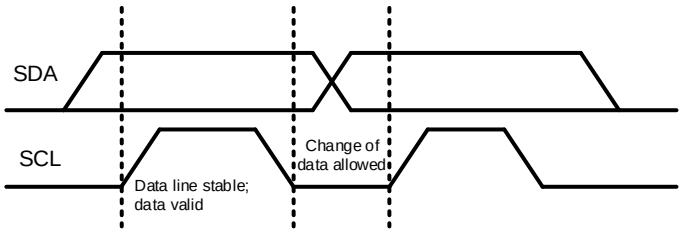


Figure 18. Bit Transfer on the I2C Bus

All the transactions begin with a START(S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition (see Figure 19).

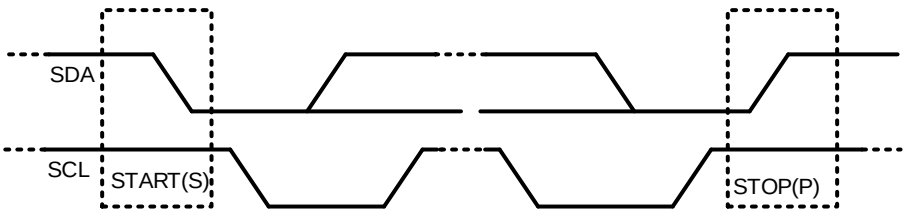


Figure 19. START and STOP Conditions

Every byte on the SDA line must be 8 bits long. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL (see Figure 20).

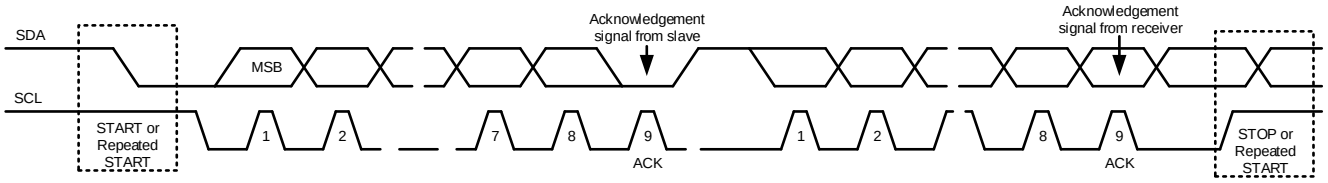


Figure 20. Data Transfer on the I2C Bus

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse, so the receiver can pull the SDA line LOW. The SDA line remains HIGH during the 9th clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer. After the START, a slave address is sent. This address is 7 bits long followed by the 8th a data direction bit (bit R/W), A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The complete data transfer is shown in Figure 21. If the register address is not defined, GD30WS8663 sends back NACK and go back to the idle state. GD30WS8663 supports single-write and single-read, shown in Figure 22 and Figure 23.

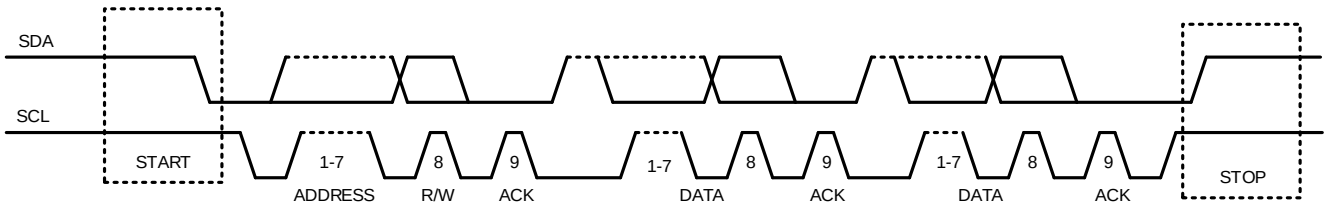


Figure 21. Complete Data Transfer

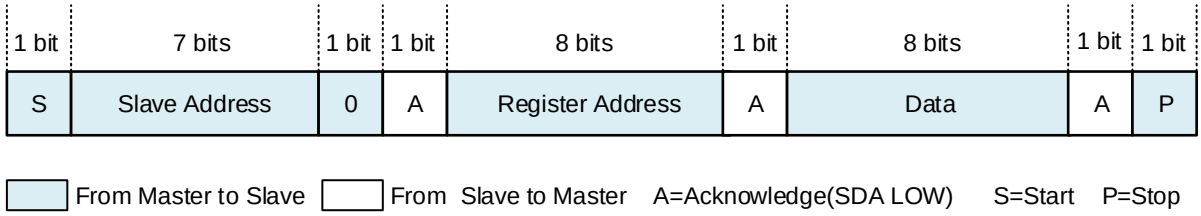


Figure 22. Single Write

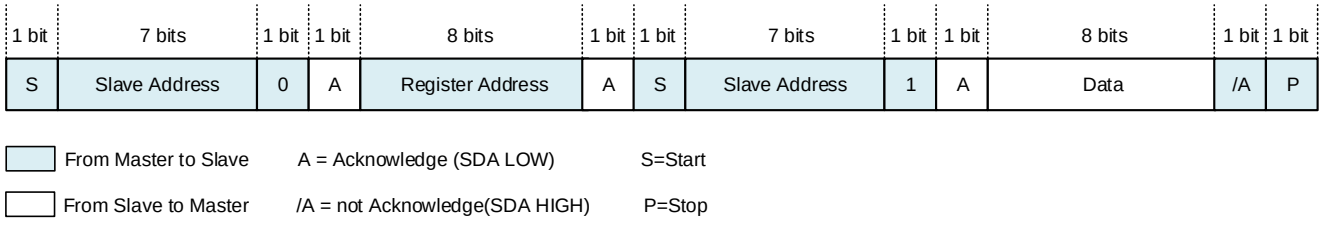


Figure 23. Single Read

6.6 Register Map

REGISTER NAME	ADDRESS	R/W	DESCRIPTION	DEFAULT
REG00H	0x00	r/w	Input source control	1001 1111
REG01H	0x01	r/w	Power on configuration register	1010 1100
REG02H	0x02	r/w	Charge current control register	0000 1111
REG03H	0x03	r/w	Discharge/termination current	1001 0001
REG04H	0x04	r/w	Charge voltage control	1010 0011
REG05H	0x05	r/w	Charge termination/timer control register	0111 1010
REG06H	0x06	r/w	Miscellaneous operation control	1100 0000
REG07H	0x07	r/w	System voltage regulation register	0011 0111
REG08H	0x08	r/w	System status register	0000 0000
REG09H	0x09	r	Fault register	0000 0010
REG0AH	0x0A	r/w	Address register	1110 0000
REG0BH	0x0B	r/w	Additional Function Control	0000 0001
REG0CH	0x0C	r/w	Additional Function Control	0000 0000

6.6.1 REG00H

Default: 1001 1111

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	V_{BUS_MIN} [3]	1	Y	N	r/w	640mV	Offset: 3.88V Range: 3.88V - 5.08V Default: 4.60V (1001)
6	V_{BUS_MIN} [2]	0	Y	N	r/w	320mV	
5	V_{BUS_MIN} [1]	0	Y	N	r/w	160mV	
4	V_{BUS_MIN} [0]	1	Y	N	r/w	80mV	
3	I_{BUS_LIM} [3]	1	Y	N	r/w	240mA	Offset: 50mA Range: 50mA - 500mA Default: 500mA (1111)
2	I_{BUS_LIM} [2]	1	Y	N	r/w	120mA	
1	I_{BUS_LIM} [1]	1	Y	N	r/w	60mA	
0	I_{BUS_LIM} [0]	1	Y	N	r/w	30mA	

6.6.2 REG01H

Default: 1010 1100

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	t_{RST_DGL}[1]	1	Y	N	r/w	00: 8s 01: 12s 10: 16s 11: 20s	Pull INT low to disconnect the battery. Default: 16s (10)
6	t_{RST_DGL} [0]	0	Y	N	r/w		
5	t_{RST_DUR}	1	Y	Y	r/w	0: 2s 1: 4s	Battery FET is off for a period of time before auto-on Default: 4s (1)
4	EN_HIZ[1]	0	Y	Y	r/w	0: Disable 1: Enable	Default: Disable (0)
3	CEB	1	Y	Y	r/w	0: Charge enable 1: Charge disabled	Charge configuration Default: charge disabled (1)
2	V_{BAT_UVLO} [2]	1	Y	Y	r/w	400mV	Battery UVLO threshold Offset: 2.45V Range: 2.45V - 3.15V Default: 2.85V (100)
1	V_{BAT_UVLO} [1]	0	Y	Y	r/w	200mV	
0	V_{BAT_UVLO} [0]	0	Y	Y	r/w	100mV	

1. This bit only controls the on and off function of the LDOFET(Q1).

6.6.3 REG02H

Default: 0000 1111

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	Register Reset	0	Y	N	r/w	0: Keep current setting 1: Reset	Default: Keep current register setting (0)
6	I2C Watchdog Timer Reset	0	Y	N	r/w	0: Normal 1: Reset	Default: Normal (0)
5	I_{CC} [5]	0	Y	Y	r/w	256mA	Constant charge current setting. Offset: 8mA Range: 8mA (000000) - 456mA (111000) Default: 128mA (001111)
4	I_{CC} [4]	0	Y	Y	r/w	128mA	
3	I_{CC} [3]	1	Y	Y	r/w	64mA	
2	I_{CC} [2]	1	Y	Y	r/w	32mA	
1	I_{CC} [1]	1	Y	Y	r/w	16mA	
0	I_{CC} [0]	1	Y	Y	r/w	8mA	

6.6.4 REG03H

Default: 1001 0001

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	I_{DSG}[3]	1	Y	Y	r/w	1600mA	BAT to SYS discharge current limit. Offset: 200mA Range: 400mA - 3.2A Valid range: 0001 - 1111 Default: 2000mA (1001)
6	I_{DSG}[2]	0	Y	Y	r/w	800mA	
5	I_{DSG}[1]	0	Y	Y	r/w	400mA	
4	I_{DSG}[0]	1	Y	Y	r/w	200mA	
3	I_{TERM} [3]	0	Y	Y	r/w	16mA	Termination current. Offset: 1mA Range: 1mA - 31mA Default: 3mA (0001)
2	I_{TERM} [2]	0	Y	Y	r/w	8mA	
1	I_{TERM} [1]	0	Y	Y	r/w	4mA	
0	I_{TERM} [0]	1	Y	Y	r/w	2mA	

6.6.5 REG04H

Default: 1010 0011

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	V_{BAT_REG} [5]	1	Y	Y	r/w	480mV	Battery regulation voltage. Offset: 3.60V Range: 3.60V - 4.545V Default: 4.2V (101000)
6	V_{BAT_REG} [4]	0	Y	Y	r/w	240mV	
5	V_{BAT_REG} [3]	1	Y	Y	r/w	120mV	
4	V_{BAT_REG} [2]	0	Y	Y	r/w	60mV	
3	V_{BAT_REG} [1]	0	Y	Y	r/w	30mV	
2	V_{BAT_REG} [0]	0	Y	Y	r/w	15mV	
1	V_{BAT_PRE}	1	Y	Y	r/w	0: 2.8V 1: 3.0V	Pre-charge to constant charge threshold. Default: 3.0V (1)
0	V_{RECH}	1	Y	Y	r/w	0: 100mV 1: 200mV	Battery recharge threshold (below V_{BAT_REG}). Default: 200mV (1)

6.6.6 REG05H

Default: 0111 1010

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	EN_WD_DISCHG	0	Y	N	r/w	0: Disable 1: Enable	Watchdog control in discharge mode. Default: Disable (0)
6	WATCHDOG [1]	1	Y	N	r/w	00: Disable timer 01: 40s 10: 80s 11: 160s	I2C watchdog timer limit. Default:160s (11) If Bit [6:5] = 00, then watchdog timer is disabled regardless of whether Bit [7] is set or not.
5	WATCHDOG [0]	1	Y	N	r/w		
4	EN_TERM	1	Y	Y	r/w	0: Disable 1: Enable	Termination setting (controlling the termination is allowed or not). Default: Enable (1)
3	EN_TIMER	1	Y	Y	r/w	0: Disable 1: Enable	Safety timer setting. Default: Enable timer (1)
2	CHG_TMR [1]	0	Y	Y	r/w	00: 3hrs 01: 5hrs 10: 8hrs 11: 12hrs	Constant charge timer. Default: 5hrs (01)
1	CHG_TMR [0]	1	Y	Y	r/w		
0	TERM_TMR	0	Y	Y	r/w	0：Disable 1：Enable	Termination timer control (when TERM_TMR is enabled, the IC will not suspend the charge current after the charge termination).

6.6.7 REG06H

Default: 1100 0000

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	EN_NTC	1	Y	Y	r/w	0: Disable 1: Enable	Default: Enable (1)
6	TMR2X_EN	1	Y	Y	r/w	0: Disable 2X extended safety timer during PPM 1: Enable 2X extended safety timer during PPM	Default: Enable (1)
5	FET_DIS[1]	0	Y	N	r/w	0: Enable 1: Turn off	Default: Enable (0)
4	PG_INT_Control	0	Y	Y	r/w	0: No Mask 1: Mask	Default: No Mask (0)
3	EOC_INT_Control	0	Y	Y	r/w	0: No Mask 1: Mask	Charge completed INT mask control Default: No Mask (0)
2	CHG STATUS_ INT_Control	0	Y	Y	r/w	0: No Mask 1: Mask	Charging status change INT mask control (charging status contain: not charging, pre charge and charge). Default: No Mask (0)
1	NTC_INT_Control	0	Y	Y	r/w	0: No Mask 1: Mask	Default: No Mask (0)
0	BATOVP_INT_ Control	0	Y	Y	r/w	0: No Mask 1: Mask	Default: No Mask (0)

1. This bit only control the turn off function of the battery FET, including charge and discharge.

6.6.8 REG07H

Default: 0011 0111

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	EN_PCB_OTP	0	Y	Y	r/w	0: Enable 1: Disable	Default: Enable (0)
6	EN_VBUSLOOP	0	Y	Y	r/w	0: Enable 1: Disable	Default: Enable (0)
5	T_{J_REG} [1]	1	Y	Y	r/w	00: 60°C 01: 80°C 10: 100°C 11: 120°C	Thermal regulation threshold. Default: 120°C (11)
4	T_{J_REG} [0]	1	Y	Y	r/w		
3	V_{SYS_REG} [3]	0	Y	Y	r/w	400mV	System voltage regulation. Offset: 4.2V Range: 4.2V - 4.95V Default: 4.55V (0111)
2	V_{SYS_REG} [2]	1	Y	Y	r/w	200mV	
1	V_{SYS_REG} [1]	1	Y	Y	r/w	100mV	
0	V_{SYS_REG} [0]	1	Y	Y	r/w	50mV	

6.6.9 REG08H

Default: 0000 0000

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	WATCHDOG_FAULT	0	Y	N/A	r	0: Normal 1: Watchdog timer expiration	Default: Normal (0)
6	NO_IN_ILIM	0	N	N	r/w	0: Use IN_ILIM 1: Disable IN_ILIM	Default: Use (0)
5	ILIM_ADD200mA	0	N	N	r/w	0: Normal IN_ILIM 1: Add 200mA	Default: Normal (0)
4	CHG_STAT [1]	0	N/A	N/A	r	00: Not charging 01: Pre charge 10: Charge 11: Charge done	Default: Not charging (00)
3	CHG_STAT [0]	0	N/A	N/A	r		
2	PPM_STAT	0	N/A	N/A	r	0: No PPM 1: In PPM	Default: No PPM (0)
1	PG_STAT	0	N/A	N/A	r	0: Power fail 1: Power good	Default: No power good (0)
0	THERM_STAT	0	N/A	N/A	r	0: No thermal regulation 1: In thermal regulation	Default: Normal (0)

6.6.10 REG09H

Default: 0000 0010

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	EN_SHIPPING_DGL[1]	0	Y	N	r/w	00: 1s 01: 2s 10: 4s 11: 8s	Enter shipping mode deglitch time Default: 1s (00)
6	EN_SHIPPING_DGL[0]	0	Y	N	r/w		
5	V_{BUS}_FAULT	0	N/A	N/A	r	0: Normal 1: V_{BUS} fault (OVP or bad source)	Default: Normal (0)
4	THEM_SD	0	N/A	N/A	r	0: Normal 1: Thermal shutdown	Default: Normal (0)
3	BAT_FAULT	0	N/A	N/A	r	0: Normal 1: Battery OVP	Default: Normal (0)
2	STMR_FAULT	0	N/A	N/A	r	0: Normal 1: Safety timer expiration	Default: Normal (0)
1	NTC_STATE[1]	1	N/A	N/A	r	00: NTC Cold > 76% (<0°C) 01: NTC Cool 76%-61% (0°C~15°C) 10: NTC Normal 61%-30% (15°C~45°C) 11: NTC hot < 30% (>45°C)	Default: Normal (10)
0	NTC_STATE[0]	0	N/A	N/A	r		

6.6.11 REG0AH

Default: 1110 0000

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	ADDR[2]	1	N/A	N/A	r/w	001:01H 010:02H 011:03H 100:04H 101:05H 110:06H 111:07H	Default: IC Address 07H (111)
6	ADDR[1]	1	N/A	N/A	r/w		
5	ADDR[0]	1	N/A	N/A	r/w		
4	Reserved	0	N/A	N/A	N/A	N/A	N/A
3	Reserved	0	N/A	N/A	N/A	N/A	N/A
2	Reserved	0	N/A	N/A	N/A	N/A	N/A
1	Reserved	0	N/A	N/A	N/A	N/A	N/A
0	Reserved	0	N/A	N/A	N/A	N/A	N/A

6.6.12 REG0BH

Default: 0000 0001

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	INT Pull-Down time	0	Y	Y	r/w	0: 256μs 1: 2.56ms	Outputting a 2.56ms low-state INT pulse. Default: 256μs (0)
6	ITERMDEG	0	Y	Y	r/w	Charge termination current deglitch time: 0: 3s 1: 1s	Default: 3s (0)
5	PRETO	0	Y	Y	r/w	0: Pre-charge timeout is 1h 1: Pre-charge timeout is 2h	Default: 1h (0)
4	DIS_SHIPINT	0	Y	Y	r/w	The function of disabling INT PIN during SHIPPING mode: 0: Nominal INT PIN function 1: Disable INT PIN function during SHIPPING mode.	Default: Normal (0)
3	Reserved	0	N/A	N/A	N/A		
2	INT100MS	0	Y	Y	r/w	INT 100ms exit shipping mode 0: 2s 1: 100ms	Default: 2s (0)
1	t_{RST_DUR}	0	Y	Y	r/w	0: Nominal t_{RST_DUR} 1: 100ms	Battery FET is off for a period of time before auto-on Default: 2s or 4s (0)
0	EN_SHIPMD_0P1S	1	Y	Y	r/w	VIN Plug：In deglitch time of shipping mode out: 0: 2s; 1: 100ms	Default: 100ms (1)

6.6.13 REG0CH

Default: 0000 0000

BIT	NAME	POR	Reset by REG_RST	Reset by WTD	R/W	DESCRIPTION	COMMENT
7	Reserved	0	N/A	N/A	N/A	N/A	N/A
6	Reserved	0	N/A	N/A	N/A	N/A	N/A
5	Reserved	0	N/A	N/A	N/A	N/A	N/A
4	Reserved	0	N/A	N/A	N/A	N/A	N/A
3	COLD_RESET	0	N/A	N/A	r/w	BATFET Reset： 0: Not Reset BATFET 1: Reset BATFET	Auto cleared after BATFET Reset Default: Reset (0)
2	DIS_VDD	0	Y	Y	r/w	0: Enable Battery Power 1: Disable Battery Power	VDD Output Voltage Pin Setting Default: Enable (0)
1	Reserved	0	N/A	N/A	N/A	Reserved	
0	CC_FINE	0	Y	Y	r/w	0: Keep default I_{CC} as I_{CC}[5:0] defined 1: Program I_{CC} with all specs of I_{CC}[5:0] divided by 4.	Finer turn charge current Default: Keep (0)

7 Application Information

A typical application of the GD30WS8663 consists of the device configured as an I2C controlled single cell Li-ion battery charger and power path manager or small battery applications such as smart-watches and wireless headsets. A battery thermistor may be connected to the NTC pin to allow the device to monitor the battery temperature and control charging as desired.

The system designer may connect the INT to the host to send a charging status and fault interrupt signal. INT is also used to disconnect the system from the battery or to allow the application's end user to reset the system. If not used this pin must be tied to BAT.

7.1 Typical Application Circuit

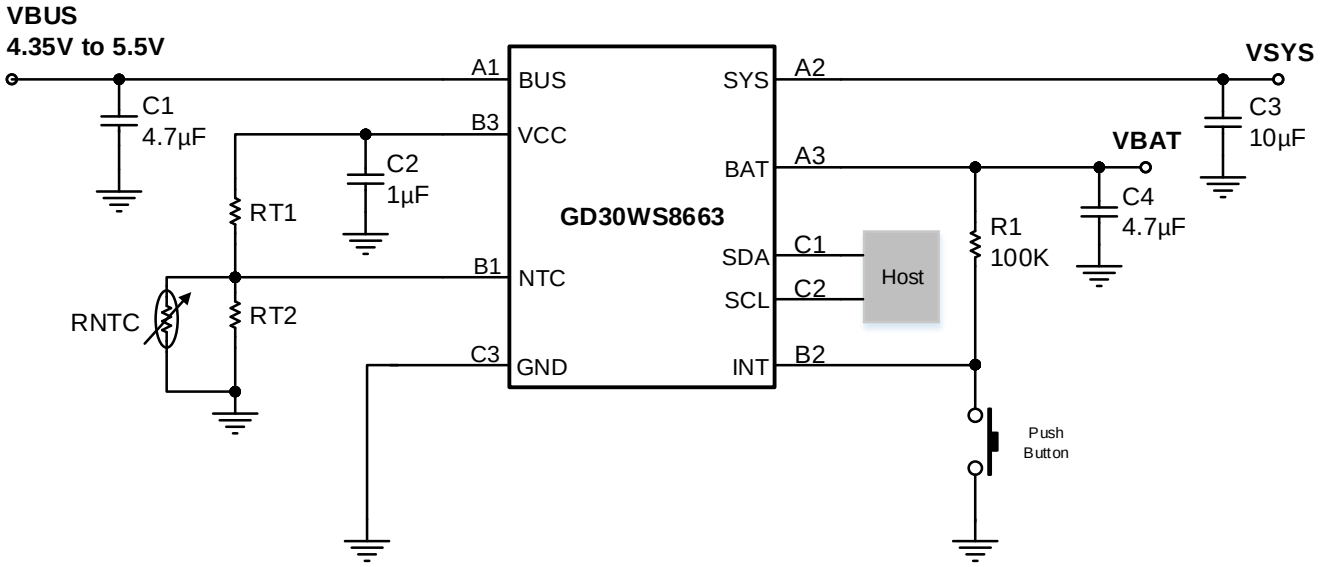


Figure 24. GD30WS8663 Recommended Application Circuit

7.2 Design Example

For this design example, use the parameters in Table 6.

Table 6. Design Parameters

PARAMETER	EXAMPLE VALUE
Input Voltage	5V
Battery Regulation Voltage	4.2V
LDO Output Voltage	3.3V

7.3 Detailed Design Description

7.3.1 External Capacitor Setting

Like most low dropout regulators, the GD30WS8663 requires external capacitors for regulator stability and voltage spike immunity. Low ESR ceramic capacitors such as X7R or X5R is preferred for input decoupling capacitors and should be places as close as possible to the supply and ground pins fo the IC.

Connect a at least 4.7μF ceramic capacitor between IN to GND for stable operation over the full load current range.

The IC is designed specifically to work with a very small ceramic output capacitor. A ceramic capacitor at least 10μF is suitable for the application circuit. For the GD30WS8663, the output capacitor should be connected between SYS and GND with thick traces and a small loop area.

A at least 4.7μF ceramic capacitor from BAT to GND is suitable for the GD30WS8663 application circuit.

A capacitor between VCC and GND is used to stabilize the VCC voltage to power the internal control and logic circuit. The typical value of this capacitor is 1μF.

7.3.2 NTC Sensor Selection

The NTC pin uses a resistor divider from the input source (VDD) to sense the battery temperature. The two resistors (RT1 and RT2) allow the high temperature limit and low temperature limit to be programmed independently (see Figure 25). The IC can fit most types of NTC resistors and different temperature operation range requirements with the two extra resistors

For a given NTC thermistor, the RT1 and RT2 values depend on the type of NTC resistor used and can be calculated with Equation and Equation:

$$RT2 = \frac{(V_{CLOD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{CLOD}V_{HOT}) \times R_{NTCL} - (V_{CLOD} - V_{CLOD}V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$RT1 = \frac{1 - V_{CLOD}}{V_{CLOD}} \times (R_{T2} \parallel R_{NTCL}) \quad (2)$$

Where R_{NTCH} is the value of the NTC resistor at the high temperature of the required operating temperature range, and R_{NTCL} is the value of the NTC resistor at a low temperature.

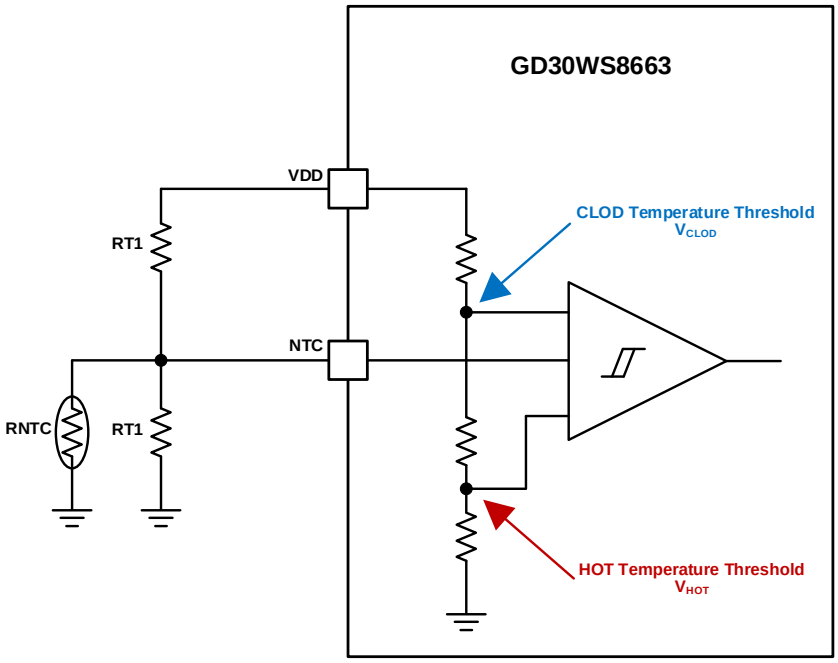
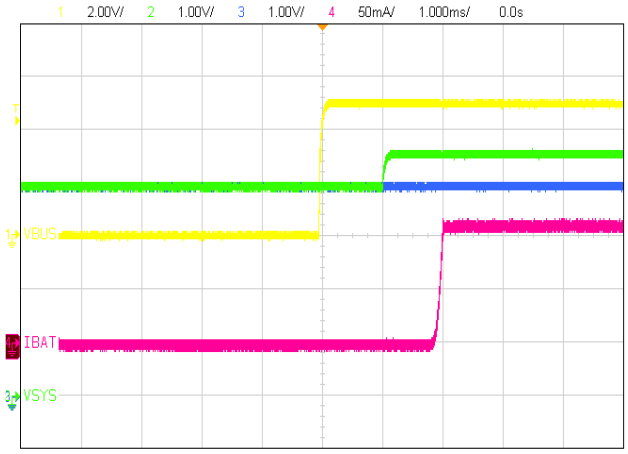


Figure 25. NTC Function Block

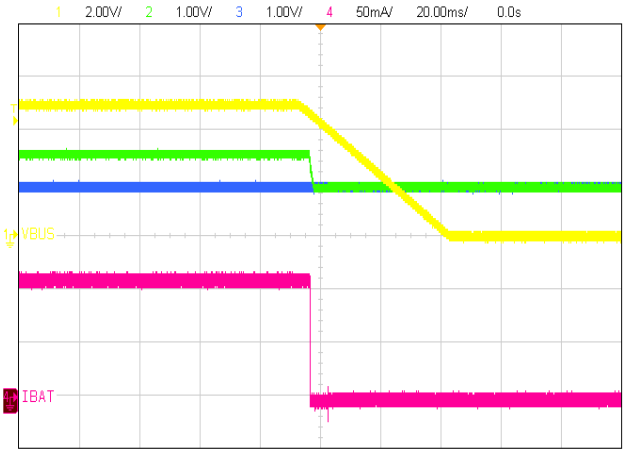
7.4 Typical Application Curves

V_{BUS} = 5V, V_{SYS} = 4.65V, V_{BAT} = 3.7V, I_{BAT} = 120mA, T_A = 25°C, unless otherwise noted.



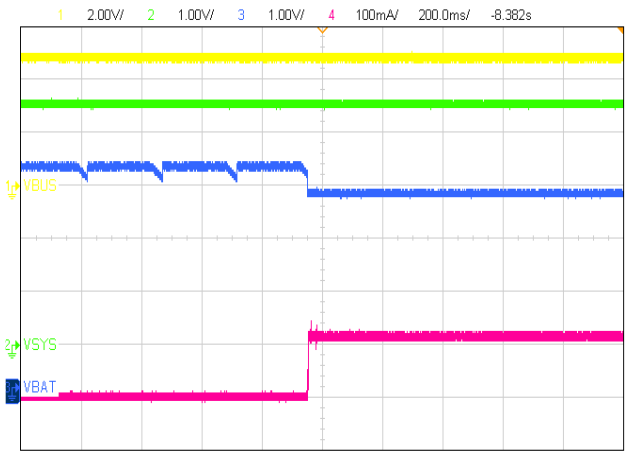
V_{BAT} = 4.0V, I_{SYS} = 0A

Figure 26. V_{BUS} Power ON



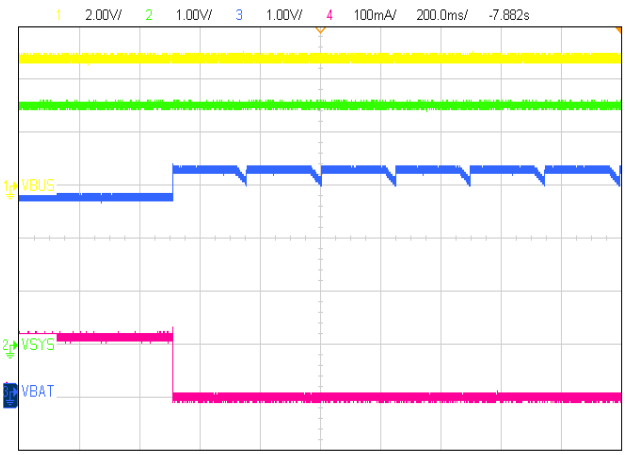
V_{BAT} = 4.0V, I_{SYS} = 0A

Figure 27. V_{BUS} Power Off



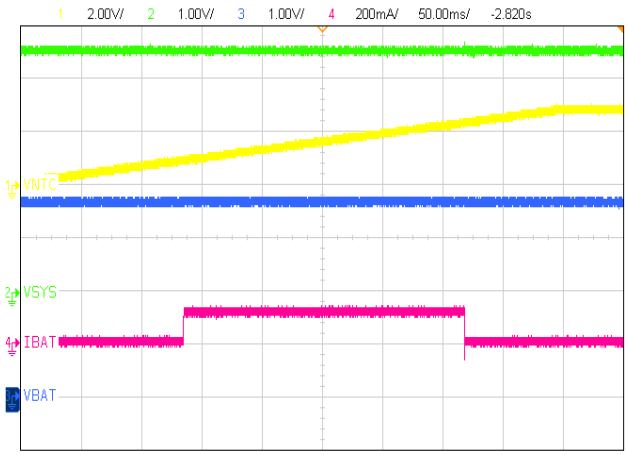
I_{SYS} = 0A

Figure 28. BAT Insertion



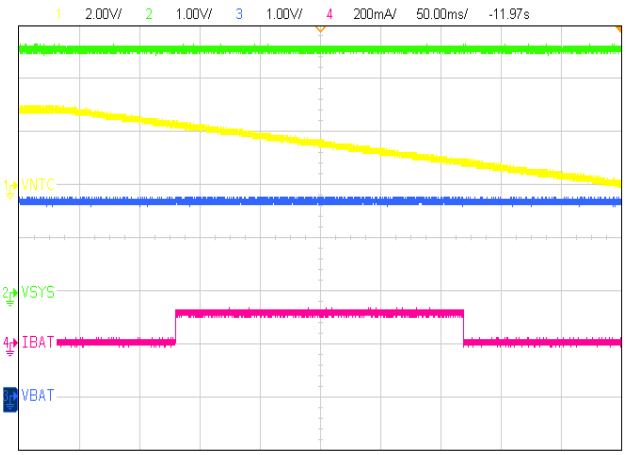
I_{SYS} = 0A

Figure 29. BAT Removal



I_{SYS} = 0A

Figure 30. NTC Rising

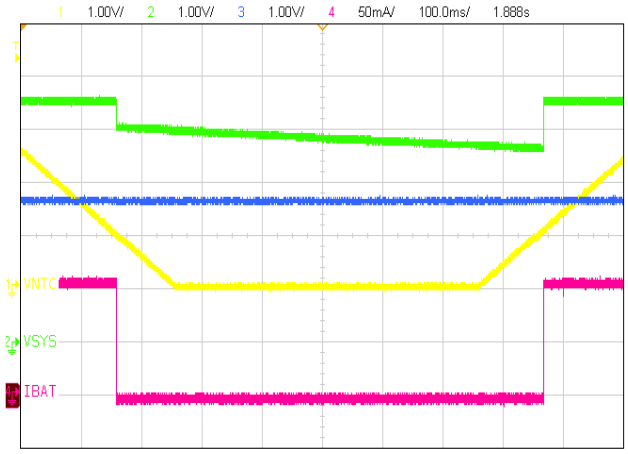


I_{SYS} = 0A

Figure 31. NTC Falling

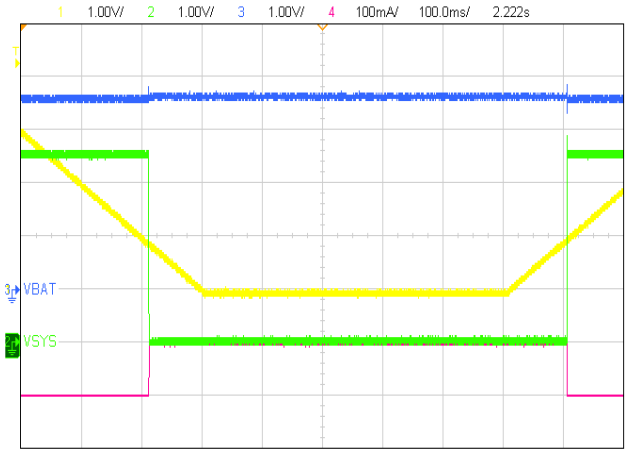
Typical Application Curves (continued)

V_{BUS} = 5V, V_{SYS} = 4.65V, V_{BAT} = 4.0V, I_{BAT} = 120mA, T_A = 25°C, unless otherwise noted.



I_{SYS} = 0A

Figure 32. PCB_OTP Charge Mode



I_{SYS} = 0A

Figure 33. PCB_OTP Discharge Mode

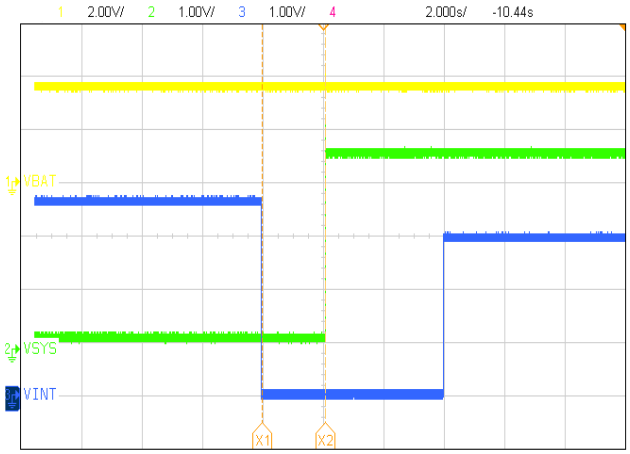


Figure 34. Exit Shipping Mode – INT Pull Down

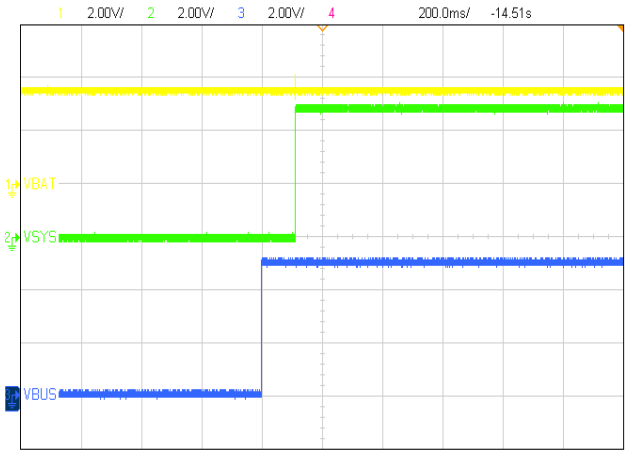
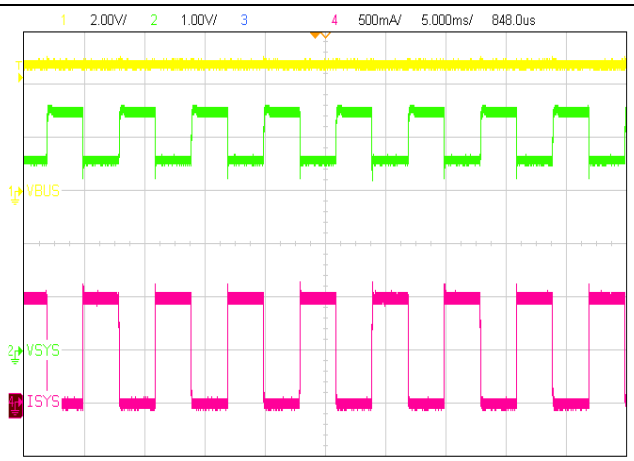
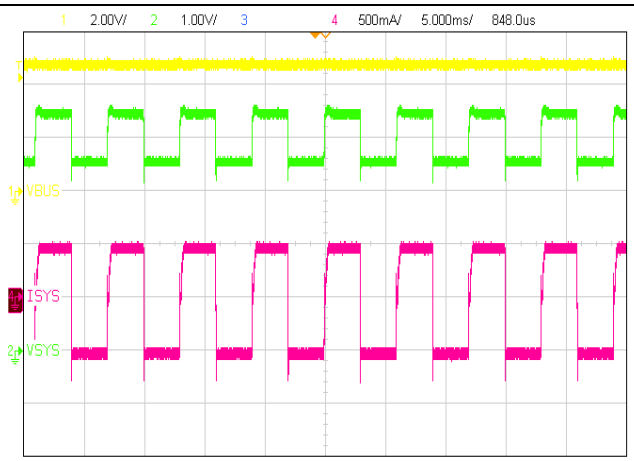


Figure 35. Exit Shipping Mode – VBUS Plug In



I_{SYS} = 0-1A, I_{BAT} = 483mA

Figure 36. SYS Load Transient 1

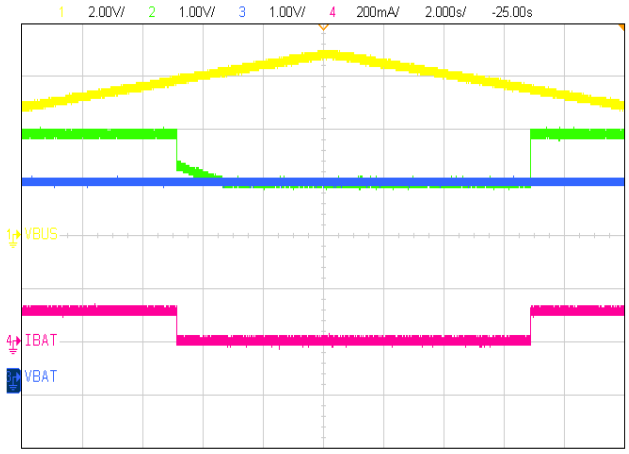


I_{SYS} = 0-1A, I_{BAT} = 483mA

Figure 37. SYS Load Transient 2

Typical Application Curves (continued)

V_{BUS} = 5V, V_{SYS} = 4.65V, V_{BAT} = 4.0V, I_{BAT} = 120mA, T_A = 25°C, unless otherwise noted.



I_{SYS} = 0A

Figure 38. VIN OVP Operation

8 Layout Guidelines and Example

8.1 Layout Guidelines

1. Place the bypass capacitors as close to the IC as possible to ensure the smallest input inductance and ground impedance.
2. Place the PCB trace connecting the capacitor between VCC and GND very close to the IC.
3. Place the I2C wire in parallel.
4. Place via in the INT pin and route from the bottom layer.

8.2 Layout Example

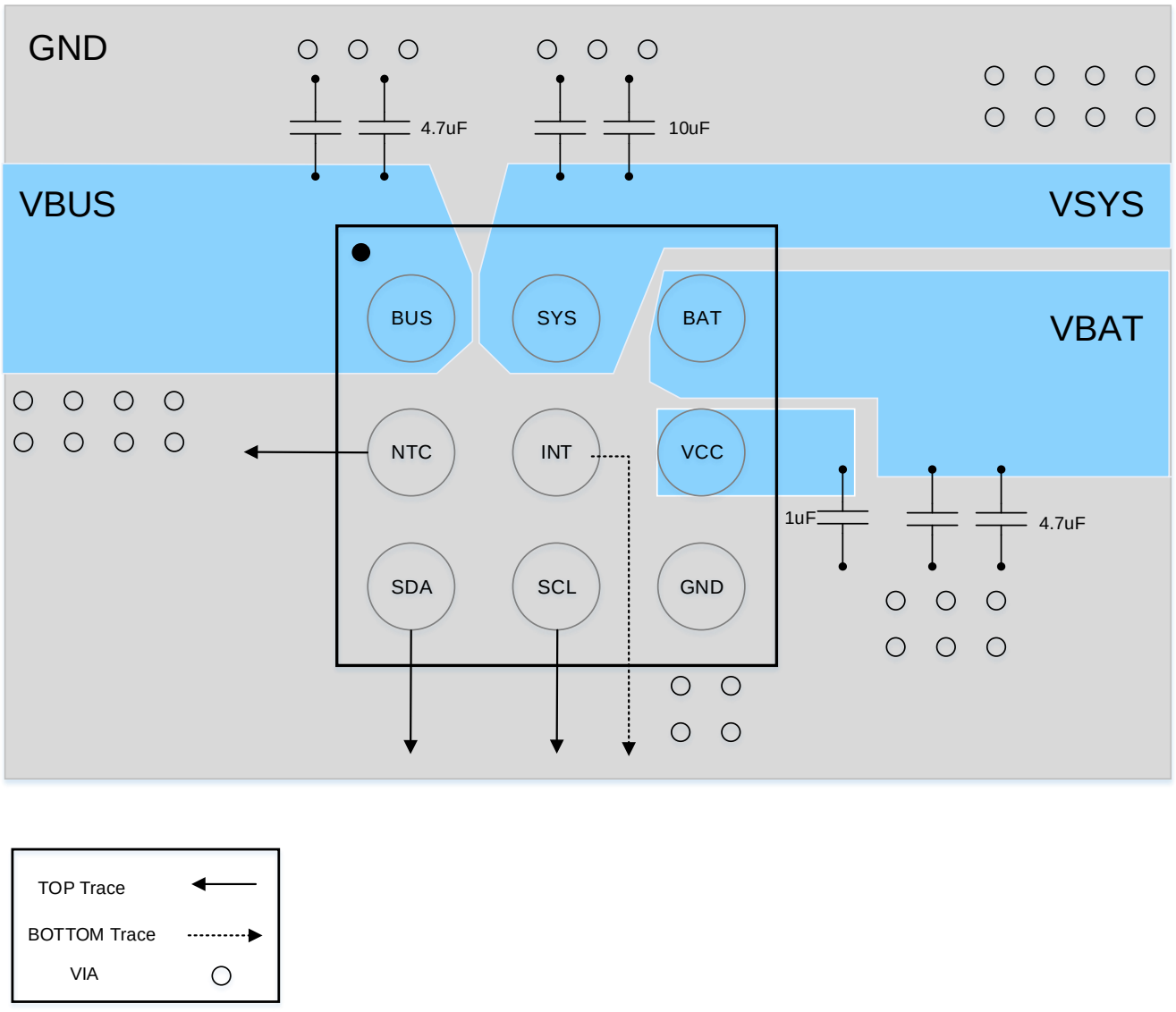
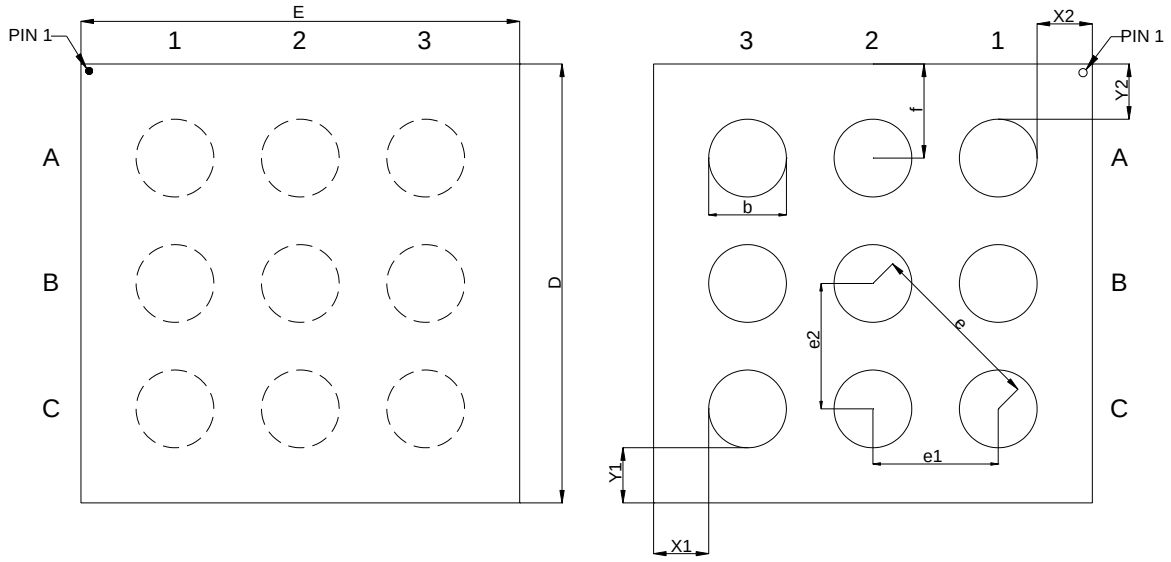


Figure 39. GD30WS8663 Layout Example

9 Package Information

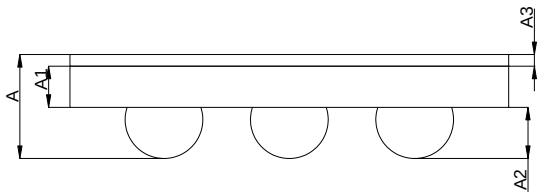
9.1 Outline Dimensions

WLCSP-9 Package Outline



TOP View

BOTTOM View



Side View

NOTES:

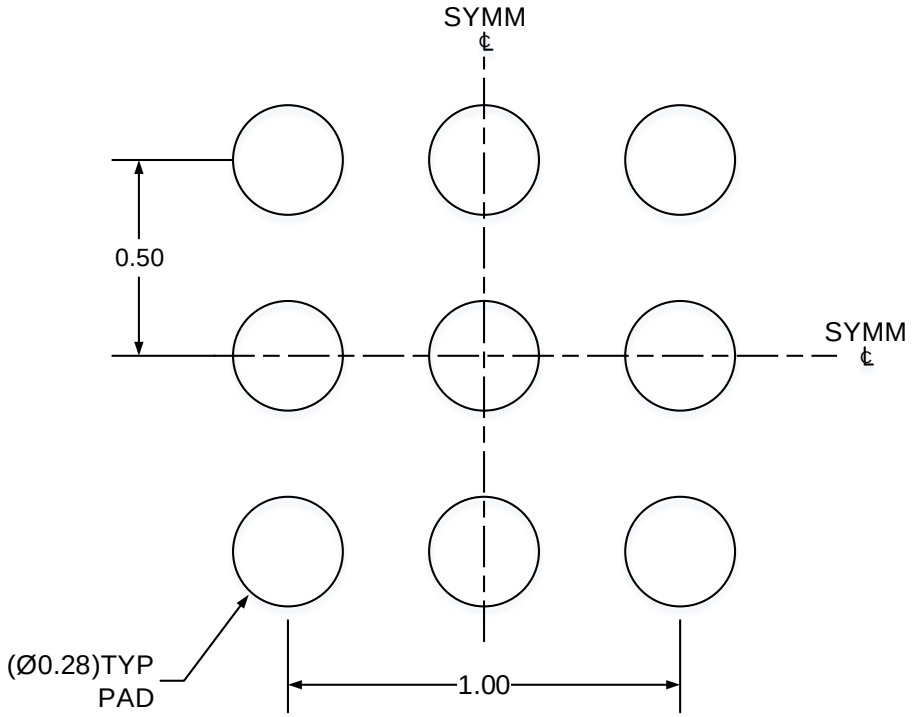
1. All dimensions are in millimeters.
2. Package dimensions does not include mold flash, protrusions, or gate burrs.
3. Refer to the Table 7 *WLCSP-9 dimensions(mm)*.

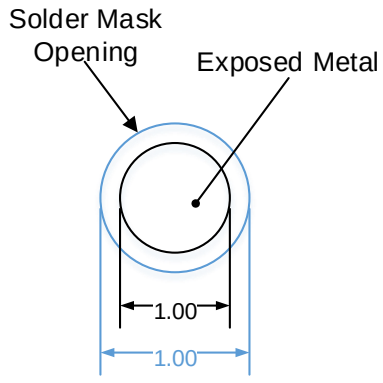
Table 7. WLCSP-9 dimensions(mm)

SYMBOL	MIN	NOM	MAX
A	0.550	0.600	0.650
A1	0.295	0.325	0.355
A2	0.230	0.250	0.270
A3		0.025	
E	1.730	1.750	1.770
D	1.730	1.750	1.770
e		0.7071	
e1		0.500	
e2		0.500	
f		0.375	
b	0.280	0.310	0.340
X1		0.220 REF	
Y1		0.220 REF	
X2		0.220 REF	
Y2		0.220 REF	

9.2 Recommended Land Pattern

WLCSP-9 Land Pattern Example





Dimension	Recommended values
Pitch	0.50
Dpad	0.28
Dsm	0.38

NOTES: (continued)

1. Refer to the IPC-7351 can also help you complete the designs.
2. Exposed metal shown.
3. Drawing is 50X scale.

10 Ordering Information

Ordering Code	Package Type	ECO Plan	Packing Type	MOQ	OP Temp(°C)
GD30WS8663DYTR-I	WLCSP-9	Green	Tape & Reel	3000	−40°C to +125°C

11 Revision History

REVISION NUMBER	DESCRIPTION	DATE
1.0	Preliminary and device details	2024
1.1	Add typical characteristic curves	2024

Important Notice

This document is the property of GigaDevice Semiconductor Inc. and its subsidiaries (the "Company"). This document, including any product of the Company described in this document (the “Product”), is owned by the Company according to the laws of the People’s Republic of China and other applicable laws. The Company reserves all rights under such laws and no Intellectual Property Rights are transferred (either wholly or partially) or licensed by the Company (either expressly or impliedly) herein. The names and brands of third party referred thereto (if any) are the property of their respective owner and referred to for identification purposes only.

The Company makes no representations or warranties of any kind, express or implied, with regard to the merchantability and the fitness for a particular purpose of the Product, nor does the Company assume any liability arising out of the application or use of any Product described in this document. Any information provided in this document is provided only for reference purposes. It is the sole responsibility of the user of this document to determine whether the Product is suitable and fit for its applications and products planned, and properly design, program, and test the functionality and safety of its applications and products planned using the Product. Unless otherwise expressly specified in the datasheet of the Product , the Product is designed, developed, and/or manufactured for ordinary business, industrial, personal, and/or household applications only, and the Product is not designed or intended for use in (i) safety critical applications such as weapons systems, nuclear facilities, atomic energy controller, combustion controller, aeronautic or aerospace applications, traffic signal instruments, pollution control or hazardous substance management; (ii) life-support systems, other medical equipment or systems (including life support equipment and surgical implants); (iii) automotive applications or environments, including but not limited to applications for active and passive safety of automobiles (regardless of front market or aftermarket), for example, EPS, braking, ADAS (camera/fusion), EMS, TCU, BMS, BSG, TPMS, Airbag, Suspension, DMS, ICMS, Domain, ESC, DCDC, e-clutch, advanced-lighting, etc.. Automobile herein means a vehicle propelled by a self-contained motor, engine or the like, such as, without limitation, cars, trucks, motorcycles, electric cars, and other transportation devices; and/or (iv) other uses where the failure of the device or the Product can reasonably be expected to result in personal injury, death, or severe property or environmental damage (collectively "Unintended Uses"). Customers shall take any and all actions to ensure the Product meets the applicable laws and regulations. The Company is not liable for, in whole or in part, and customers shall hereby release the Company as well as its suppliers and/or distributors from, any claim, damage, or other liability arising from or related to all Unintended Uses of the Product. Customers shall indemnify and hold the Company, and its officers, employees, subsidiaries, affiliates as well as its suppliers and/or distributors harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of the Product.

Information in this document is provided solely in connection with the Product. The Company reserves the right to make changes, corrections, modifications or improvements to this document and the Product described herein at any time without notice. The Company shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them. Information in this document supersedes and replaces information previously supplied in any prior versions of this document.